Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Scientific Seminar on Structure, Architecture, and Application of Sensor Circuits

Chair of Circuit Design

Summer Semester 2024

What you will learn in this seminar …

- At least 50% of this seminar is about the soft skills you need to become a successful engineer in science, but also in industry
- You will learn to:
  - Research state-of-the-art for a newly defined problem, and get a deeper understanding of the problem
  - Formulate a plan for solving the problem
  - Present technical work in a scientific paper, such that others can understand the content but also the motivation for the topic, what others have done in the field already, what you did new and better than others, as well as the remaining challenges after your work
  - Orally present the same topic to a group with the same intention

… **good work is often only recognized if it is also well presented (and for this, first of all,** it needs to be understood by others in a short time frame)!

Outline – Kick-Off Meeting

Today …

- Your work and duties during this seminar
- Timing & Deadlines: Submissions and presentations
- Grading of your work
- Presentation of topics by supervisors
- Selection of one topic per student
- Lecture: how to do research

Outline – Course of the seminar

- Then …
  - Lecture: how to write an article and to do a presentation
  - Work on your own: Text / Internet search / discussions
  - In case you need help: please contact your supervisor in advance and try to use your and his/her time efficiently
  - Take advantage of the supervisor's feedback, this is where you can learn most!
  - Show your results: report (4 pages) and oral presentation (15 min.)

Your work and duties

- Choose one of the topics
- Do research about the topic
- Write a scientific paper about the topic (4 pages)
- Prepare and give a scientific presentation (15 min + 5 min Q&A)
- For paper and presentation:
  - focus on basics of the problem and specific implementation
  - a template will be provided on Moodle

Your work and duties

1. Do a literature search and discuss your research results with your supervisor
2. Then study the literature (modified by supervisor)
3. Develop an outline (content) for your paper and presentation
4. Discuss your outline with your supervisor (by appointment)
5. Work out the (modified) outline in your paper
6. Submit your paper
7. Summarize your results in a presentation
8. Submit the presentation

Grading

- ✓ Regular discussions (online/in presence) with the assigned supervisor about the progress of the work and the procedure
- ✓ Oral presentation of the results (15 min.) with subsequent discussion (5 min.) (50%)
- ✓ Scientific paper in IEEE style (4 pages): written elaboration of the results (50%)

Timing & Deadlines

	When?	What?
Kick-off	17.04.2024 (Wednesday) 16:00-18:00	Introduction & How to do a literature research **Participation is mandatory!**
Lecture	12.06.2024 (Wednesday) 16:30-18:00	How to prepare a scientific presentation & article
Paper submission deadline	07.07.2024 (Sunday) until 23:59 PM	In Moodle and via email to your supervisor
Presentations *(planned)*	09.07.2024 (Tuesday) & 10.07.2024 (Wednesday) 16:00-18:00	

Topics (Overview)

Topic	Supervisor	Available
PLL´s with Bandwidths above fref / 10	Markus Dietl	
Audio Encoding for Spiking Neural Networks	Kilian David	
Energy-Efficient neuromorphic Hardware for Event-driven Applications	Matthias Ochs	
State-of-the-Art analyzation: Ultra-Low Power Oscillator	Tobias Chlan	
CD-Converter: Techniques, Efficiency, Flexibility	Tobias Chlan	
Evolutionary Algorithm-based Training Methods for SNN	Lei Zhang	
System-level CDM Modeling for High-Speed IO Devices	Emanuele Groppo	
ESD Diode Optimization in FinFET and GAA Technology	Emanuele Groppo	
Just a holder for the chip? - IC Packages	Carl Riehm	
Ultrasonic Sound Data Communication	Pengcheng Xu	
RF Energy Harvesting	Pengcheng Xu	
Scalability of Neuromorphic Processors	Ferdinand Pscheidl	

LAST UPDATED 02.04.2024

Supervisor: kilian.david@tum.de

Audio Encoding for Spiking Neural Networks

Hard- and Software Approach towards Electronic Ears

Problem:
Spike Generation from (Analog) Audio Source

Focus:

- Minimal Loss of relevant Information
  - SNN
  - Speech
- Delta-Modulation with Level-Crossing ADC
- Quantitatively Compare e.g.:
  - Power Consumption
  - Hardware Feasibility
  - Bandwidth

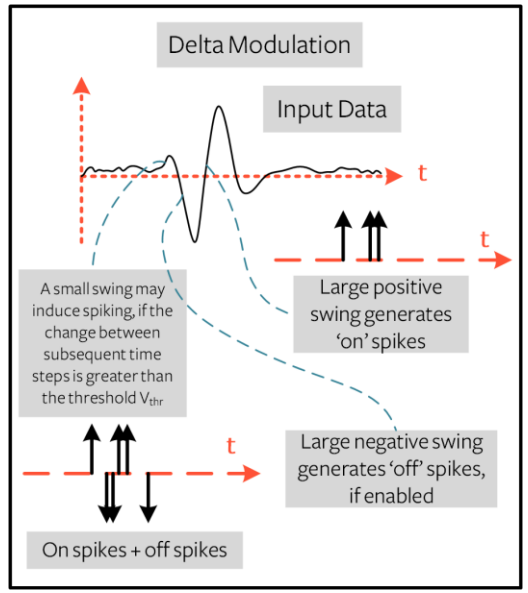


Figure 1. Delta Modulation
Source: snnTorch Tutorial 1 Jason K. Eshraghian. Revision a1d97b78.

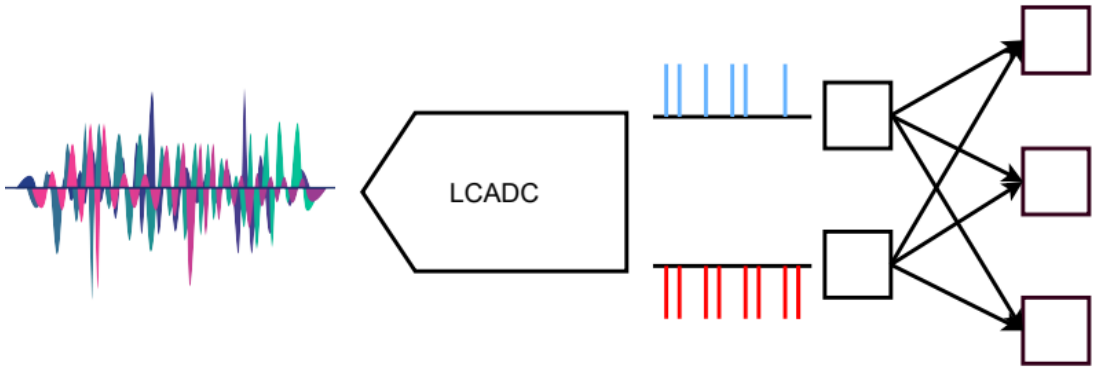
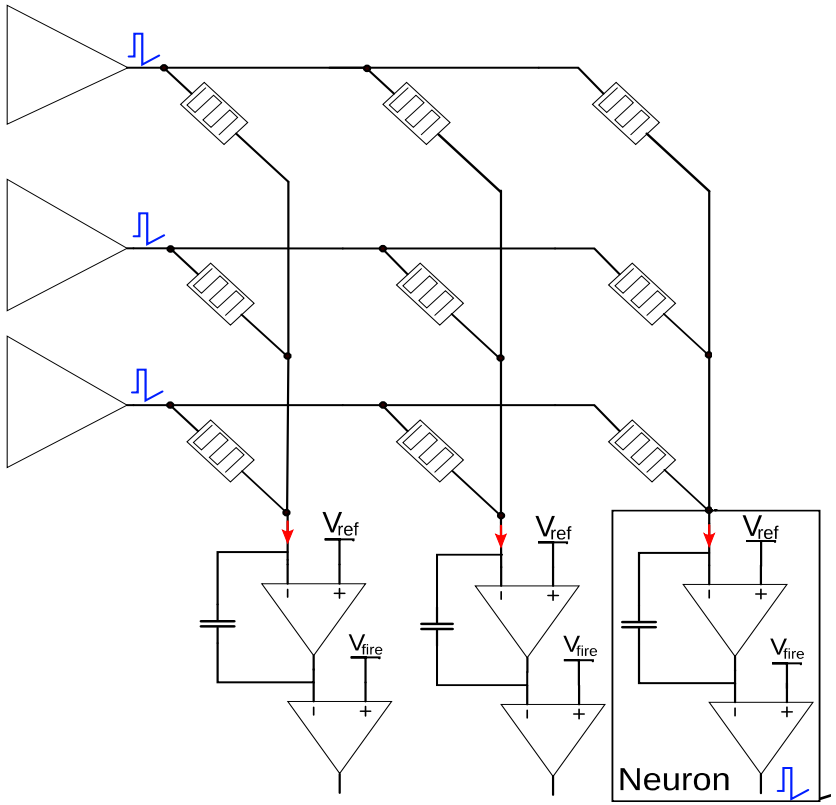


Figure 2. LCADC Spike Encoding

Y. Zhao and Y. Lian, "Event-Driven Circuits and Systems: A Promising Low Power Technique for Intelligent Sensors in AIoT Era," Jul. 2022, doi: 10.1109/TCSII.2022.3180689.

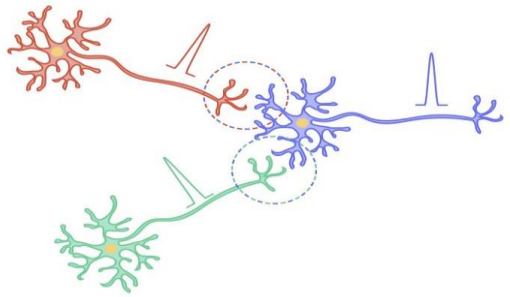
Energy-Efficient Neuromorphic Hardware for Event-Driven Applications

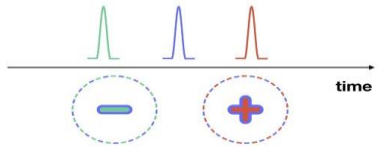
Supervisor: matthias.ochs@tum.de



SNN Crossbar with Memristive Memory

- Sensor systems at the edge (especially with battery supply) requires ultra-low-power consumption
- Sensors with low precision can use AI to classify the important information (e.g. human nose: good (delicious, sweet) or bad (poissonous, smoke) smells, action based on imprecise sensor values
- Human Brain outperforms computer systems by up to 5 decades in energy efficiency („von-Neumann-Bottleneck“)
- Spiking Neural Networks (SNN) mimic the information processing of the brain:
  - „Computing in Memory“ (Synapses store the learned information as direct connection between Neurons)
  - Sparse Events (Spikes) as information signals
  - Low precision (not necessary, but saves energy)
- **Goal is to improve energy efficiency for inference and learning by using analog HW!**





https://towardsdatascience.com/spiking-neura

Supervisor: tobias.chlan@tum.de

State-of-the-Art analyzation: Ultra-Low Power Oscillator

State-of-the-Art, Design, Comparison, Techniques

Problem:
Power consumption for 32.768kHz real-time clocks should be minimized for ultra-low-power modes: Settling, current consumption, stability

Focus

- Recent publications: ISSCC, ESSCIRC, VLSI, …
  - Overview of techniques
- State-of-the-Art: Ultra-Low-Power oscillators 32.768kHz
- Circuit Design
  - Principle, Idea
  - Analyzation of techniques
  - Understanding of regulation concepts
  - Finding of the critical system components

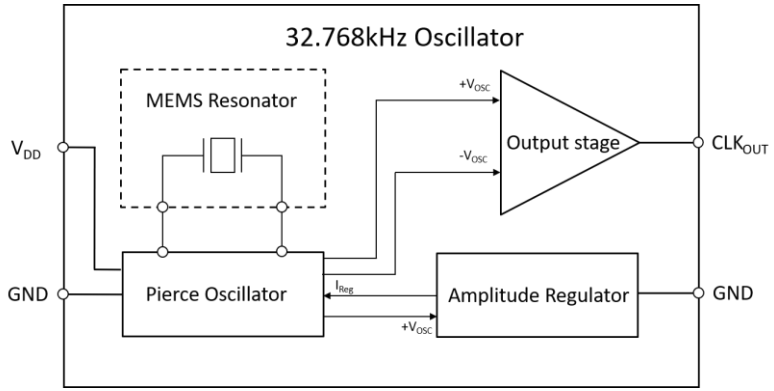


Figure 1. *Typical oscillator block diagram*

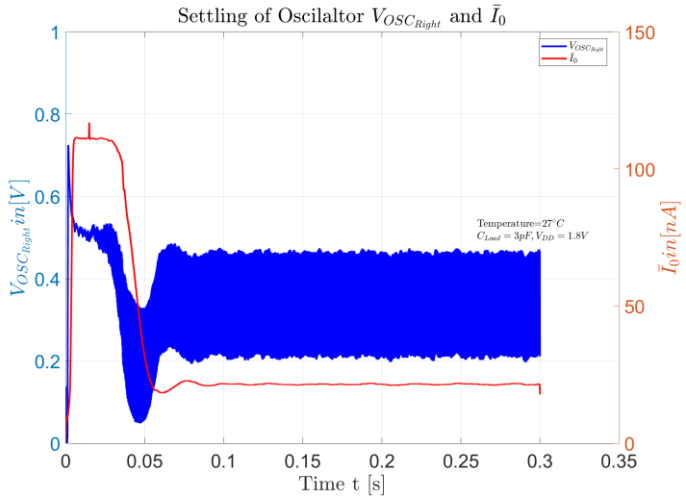


Figure 2. *Settling of an crystal/MEMS oscillator*

Supervisor: tobias.chlan@tum.de

CD-Converter: Techniques, Efficiency, Flexibility

State-of-the-Art, Design, Features, Comparison

Problem:
Need for efficient capacitance to digit converter considering topology, effort and efficiency (area, noise, current, resolution)

Focus

- State-of-the-Art: CD-Converters
  - Topologies: Delta-Sigma, SAR, Dual-Slope
  - Conversion concept? Is it directly Cap to Digit?
  - Efficiency (FoM), Resolution, …
  - Limitations of topology
- Comparison of topologies
  - Advantages/Disadvantages
  - Highlighting of the crucial trade-offs
  - Comparison table

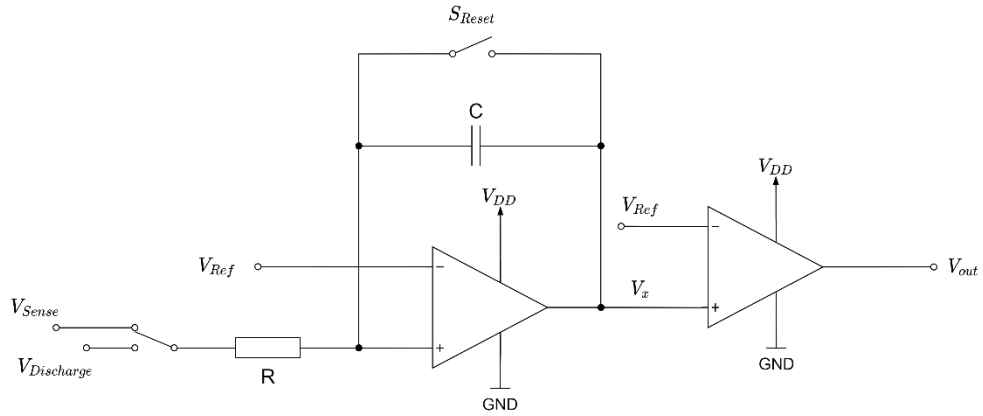


Figure 1. Dual-Slope Converter

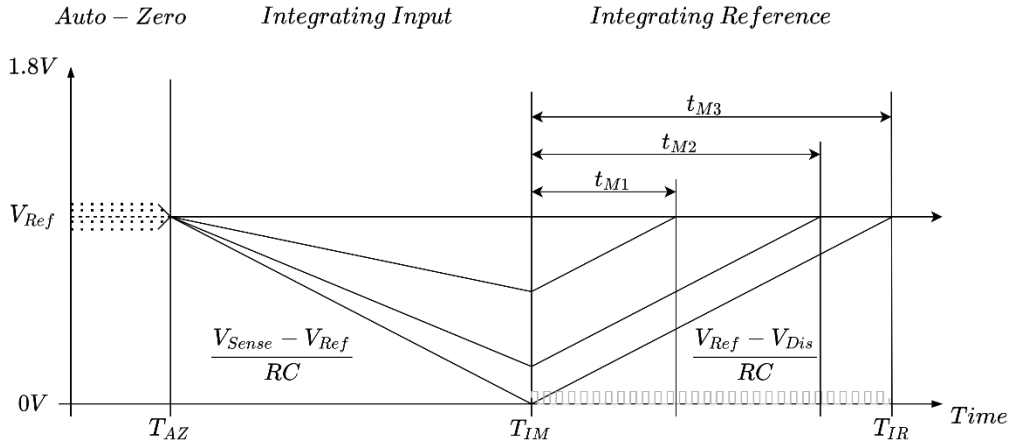


Figure 2. Typical dual-slope conversion cycle

Source Figure 1, 2: Analog-to-digital converter for the genration of keys with mechanical stress compensation, Tobias Chlan

Supervisor: lei1993.zhang@tum.de

Evolutionary Algorithm-based Training Methods for SNN

Problem:
Training spiking neural networks on the analog hardware is complicated. Our newest idea is to let analog hardware evolving by itself. This could be done using evolutionary algorithms.

Focus:

- Literature Study
  - SNN Training Methods with Evolutionary Algorithms (e.g., NEAT)
- Possible Implementation of Evolutionary Algorithms on the SNN Hardware
- Think about advantages and disadvantages

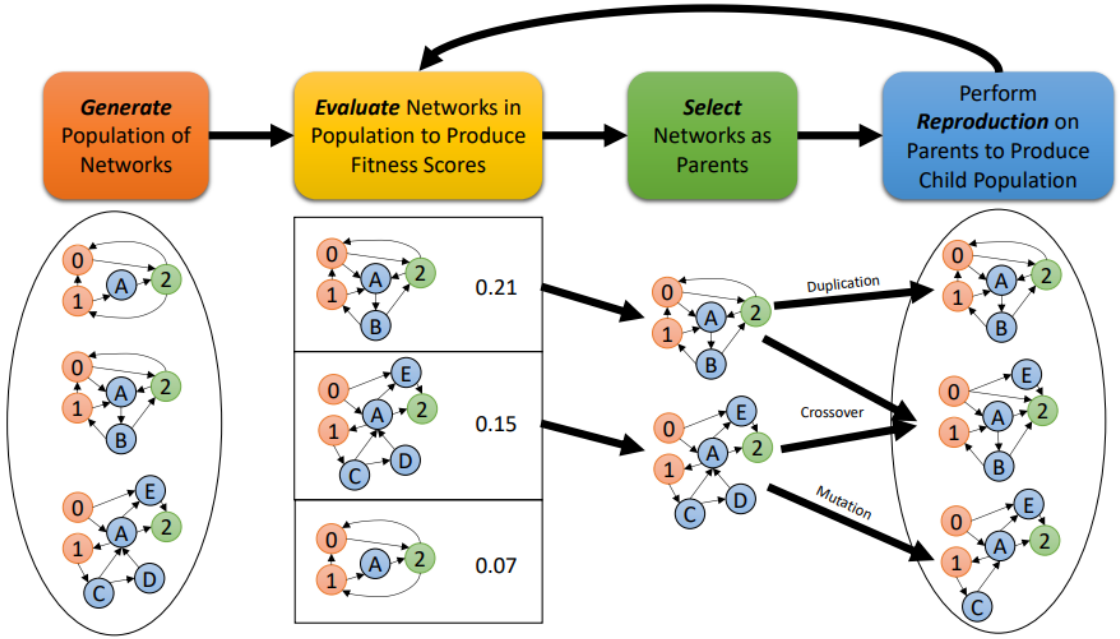


Figure 1. An example of Evolutionary Optimization for Neuromorphic Systems (EONS).

Figure 1: https://www.osti.gov/servlets/purl/1649325

Supervisor: emanuele.groppo@tum.de

System-level CDM Modeling for High-Speed IO Devices

Problem:
Modeling Charged Device Model (CDM) events for effective High-Bandwidth IO protection

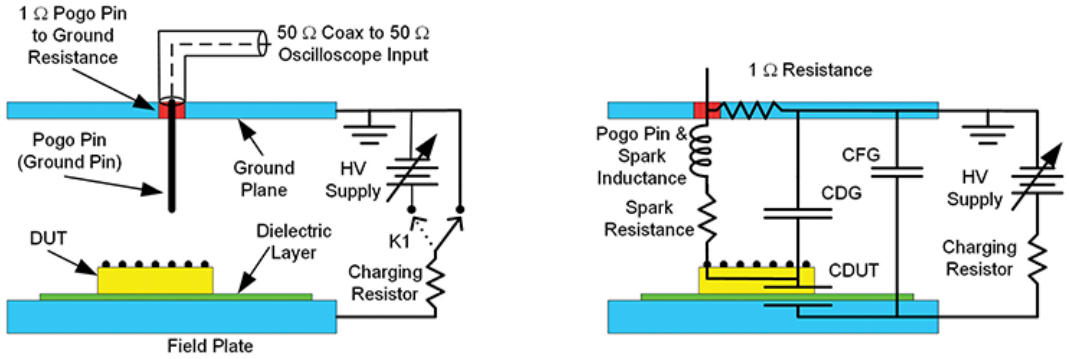


Figure 1. CDM tester schematic and equivalent circuit model.
ANSI/ESDA/JEDEC JS-002-2022. "Joint Standard for Electrostatic Discharge Sensitivity Testing – Charged Device Model (CDM) – Device Level." http://www.esda.org/standards/esda-documents.

Focus:

- State of the art review
  - Available models for CDM tester and DUT
  - Basic ESD protection networks for IO devices
  - Modeling approaches for fast-transient effects
- Behavior under fast rise time events
  - Rise-time sensitive devices
  - Impact of die and package parasitics
  - Tools and methods for optimization

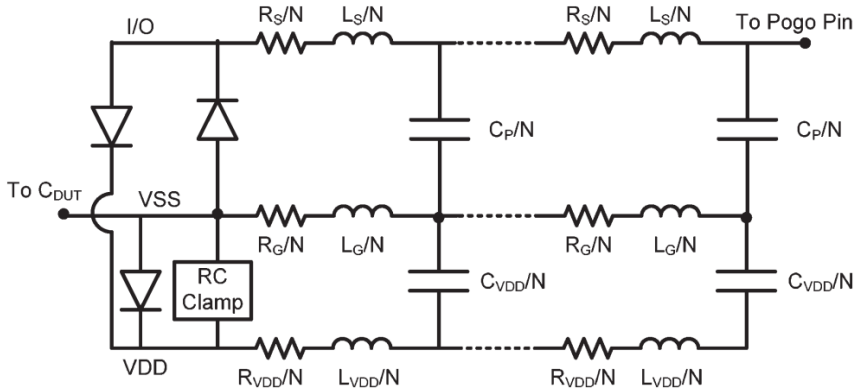


Figure 2. Example of Device Under Test modeling approach.
Di Sarro, James P., Bill Reynolds, and Robert Gauthier. "Influence of package trace properties on CDM stress." IEEE Transactions on Device and Materials Reliability 14.3 (2014): 810-817.

Supervisor: emanuele.groppo@tum.de

ESD Diode Optimization in FinFET and GAA Technology

Problem:
Missing framework for ElectroStatic Discharge (ESD) in advanced semiconductor technologies

Focus:

- State of the art review
  - FinFET and Gate-All-Around (GAA) technology
  - ESD in advanced semiconductor nodes
- Physics of ESD events
  - Current discharge path
  - Thermal behavior and constraints
- Device parameters impact
  - Tools and methods for optimization

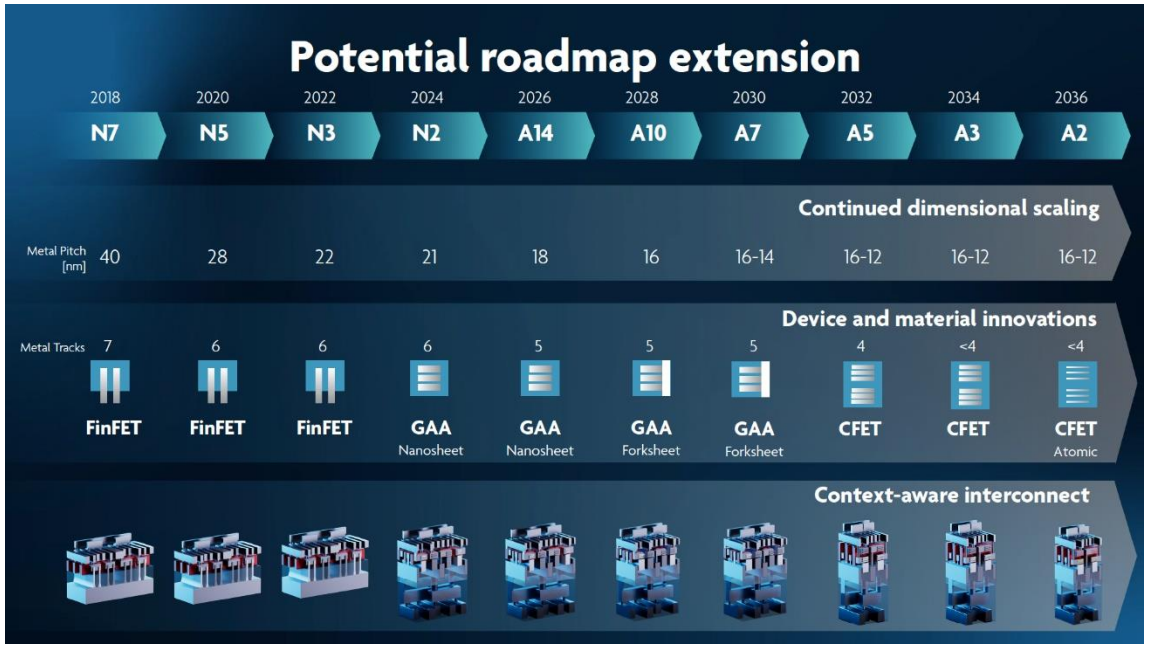


Figure 1. Semiconductor devices roadmap.
https://www.imec-int.com/en/articles/20-year-roadmap-tearing-down-walls

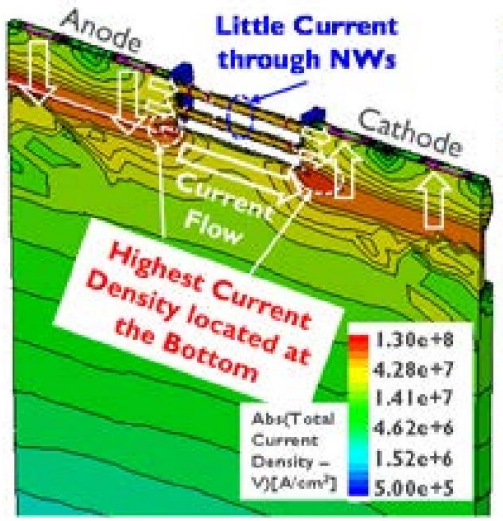


Figure 2. Current density distribution in GAA ESD diode.
Chen, S.-H., et al. "ESD Diodes in a Bulk Si Gate-All-around Vertically Stacked Horizontal Nanowire Technology." In *2016 IEEE International Electron Devices Meeting (IEDM)*, 35.4.1-35.4.4, 2016.

Supervisor: carl.riehm@tum.de

Just a holder for the chip? - IC Packages

An overview and comparison of IC packages

Problem:
Silicon dies require packaging to be used in any application. However, packaging of a chip may impact the circuit performance.

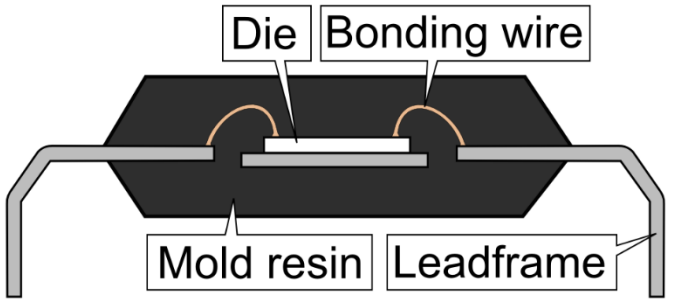


Figure 1: cross section of a dual in-line package
https://en.wikipedia.org/wiki/Integrated_circuit_packaging

Focus/Tasks (dependent on interest)

- Types of IC packages
  - What kind of packages are existing?
  - Can they be categorized?
  - What kind of advantages/disadvantages do they have?
- How is an IC package impacting chips?
  What kind of parasitic mechanisms do exist?
- IC packaging process steps

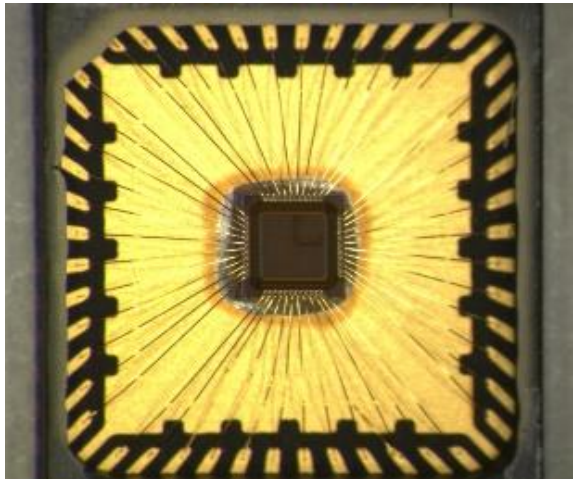
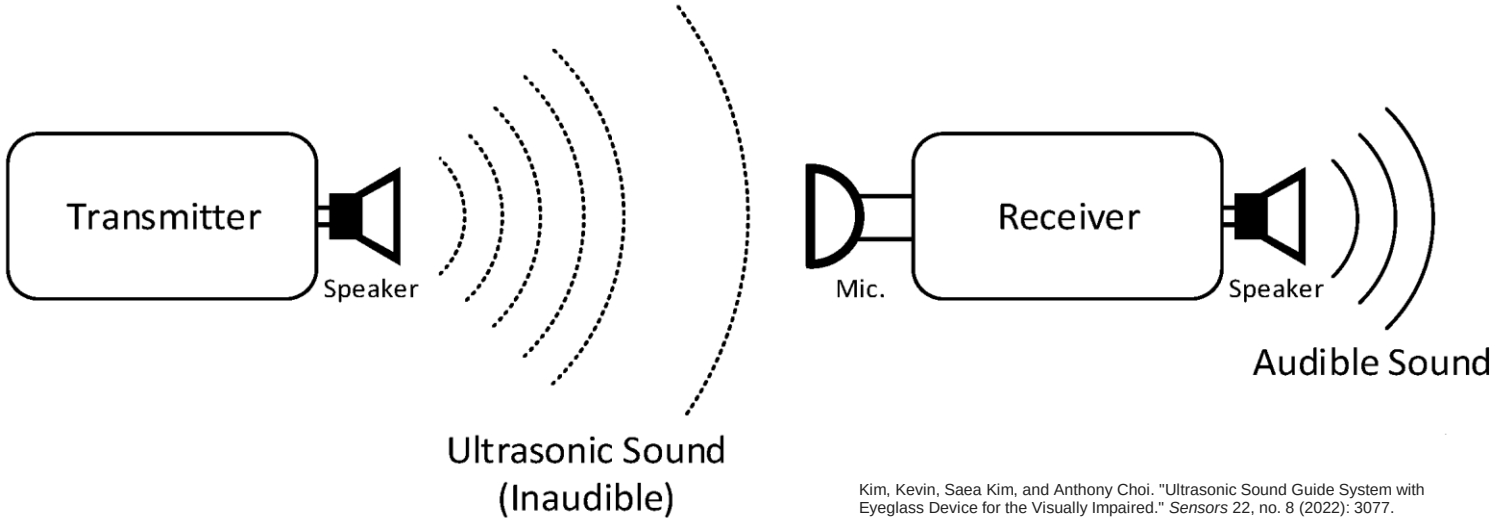


Figure 2: open TQFP package (lid removed)

Supervisor: pengcheng.xu@tum.de

Ultrasonic Sound Data Communication

State-of-the-Art Works Review



Kim, Kevin, Saea Kim, and Anthony Choi. "Ultrasonic Sound Guide System with Eyeglass Device for the Visually Impaired." *Sensors* 22, no. 8 (2022): 3077.

Focus:

- Motivation: Why we need to transmit/receive data by ultrasonic sound? For which application?
- Specifications: What is the specifications for an ultrasonic sound data communication?
- Design: What is the basic structure and circuit for an ultrasonic sound transmitter/receiver? What the state-of-the-art works for these design? What are the advantages/disadvantages for these works?
- Comparison: Compare the ultrasonic sound data communication with the conventional wire data communication, RF data communication, etc.

Figure 1: https://www.sciencedirect.com/science/article/pii/S0165993618303674

Figure 2: https://www.nature.com/articles/s41378-018-0019-0

Supervisor: pengcheng.xu@tum.de

RF Energy Harvesting

State-of-the-Art Works Review

Focus:

- Application: RF energy harvester (RFEH) is used for which applications. Compare it with the conventional power supply solution
- Design: What is the basic structure and circuit for an RFEH? What the state-of-the-art works for these designs? What are the advantages/disadvantages for these works?
- Performance: How to express the RFEH performance? How to improve it? How to unify the KPI? How to compare the state-of-the-art works?

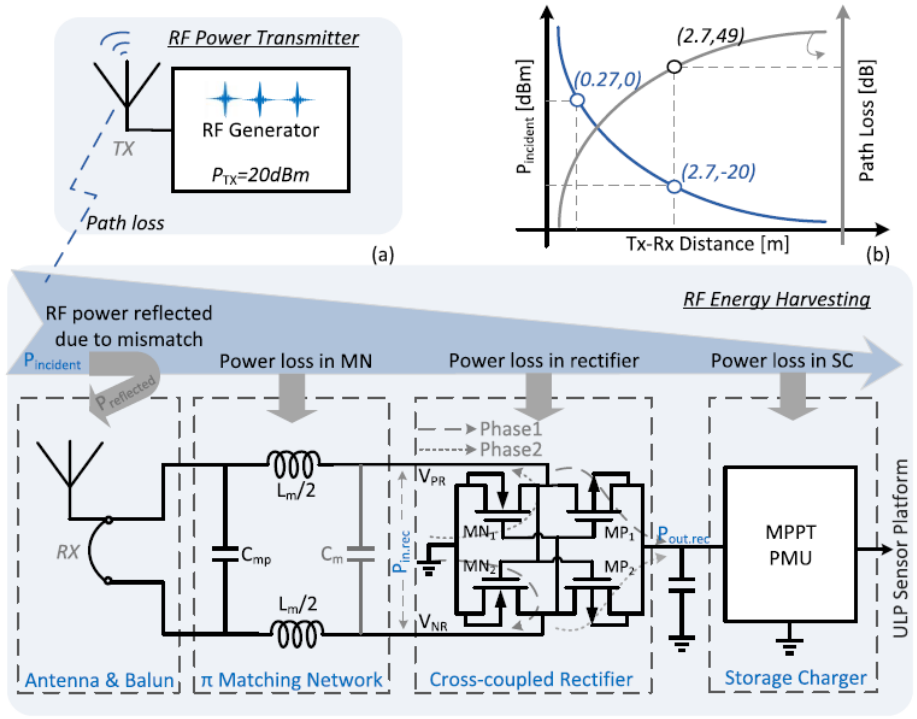


Fig. 1. RFEH for far-field WPT. (a) System architecture. (b) Link budget.

Xu, Pengcheng, Denis Flandre, and David Bol. "A self-gating RF energy harvester for wireless power transfer with high-PAPR incident waveform." *IEEE Journal of Solid-State Circuits* 56, no. 6 (2021): 1816-1826

Supervisor: ferdinand.pscheidl@tum.de

Scalability of Neuromorphic Processors

Evaluation of State-of-the-Art Architectures

Background:

One of the most important characteristic of neuromorphic processor architectures, which is affected by almost every design decision, is their scalability. On the one hand it is defined by area constraints and the density of synapses and neurons. On the other hand it is limited by functional aspects, for example the scaling of communication delays with system size.

Focus/Tasks/Goals/Structure/etc.:

- Investigate state-of-the-art neuromorphic processors
  - Investigate reported architecture characteristics
  - Investigate how these architectures would be scaled
- Estimate how typical characteristics of neuromorphic processors depend on scaling

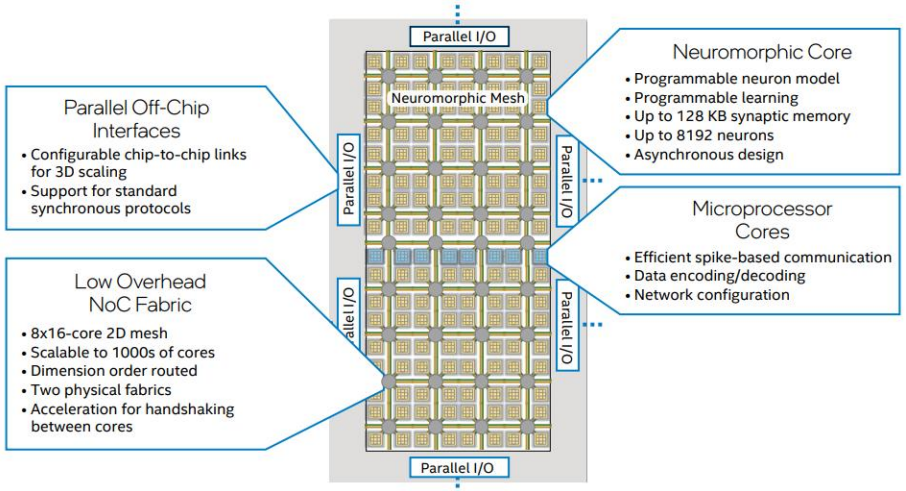


Figure 1. Loihi 2 Brief, https://www.intel.com/content/www/us/en/research/neuromorphic-computing-loihi-2-technology-brief.html , 26.03.2024

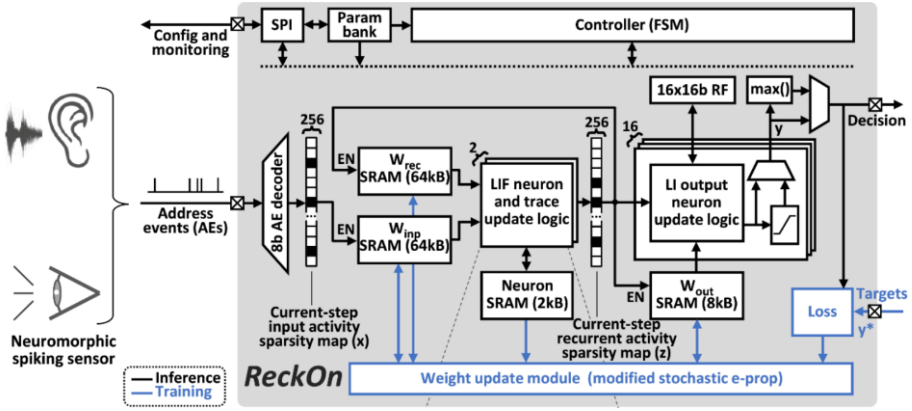


Figure 1. C. Frenkel and G. Indiveri, "ReckOn: A 28nm Sub-mm2 Task-Agnostic Spiking Recurrent Neural Network Processor Enabling On-Chip Learning over Second-Long Timescales," 2022 IEEE International Solid-State Circuits Conference (ISSCC), San Francisco, CA, USA, 2022