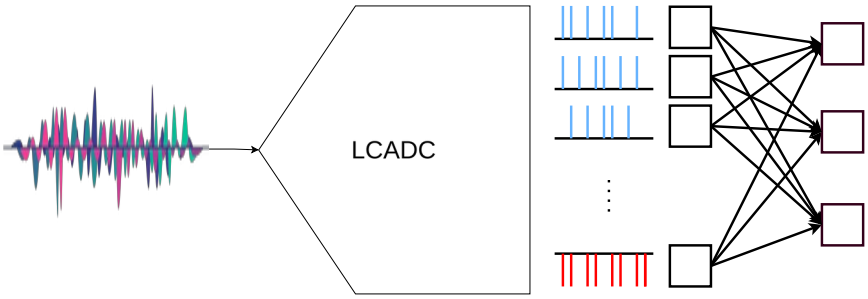
Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Design and Implementation of a multi-bit-parallel Level-Crossing ADC

Master's-Thesis at the Chair of Circuit Design
(can be combined with a research internship at the chair)

In the context of of intelligent sensor systems, spike encoding of audio signals is of high interest for the development of Spiking Neural Networks (SNN). A promising way of converting (analog) data into spikes are Level-Crossing ADCs (LCADCs). These event-driven circuits sample the input signal sparsely and thereby save power during low-activity phases.
However, during high-activity phases most LCADCs suffer from an input-signal slew-rate limit, which demands a rather high speed circuit to follow the input signal. With a resolution of n-bits, a LCADC takes 2^n steps to traverse the full input range, since each spike represents a signal change of one V_{lsb}.
The main task of this thesis consists of redesigning an existing LCADC to allow multiple binary-weighted output spikes.



Your work consists of designing and implementing the proposed design in the 22nm GF node. Both analog and digital circuit design will be done with the corresponding cadence design tools at the chair.
You will first undertake a scientific literature research on the state of the art of LCADCs in the context of SNNs. You are then free to adapt the existing design such that it meets the requirements or implement your own idea from scratch.

Familiarity with the following topics are helpful, but not mandatory:

- analog/digital circuit designing
- Virtuso, genus, Innovus
- Verilog/VHDL
- ADCs
- (Spiking) Neural Networks

Interested?	→ Contact:	Kilian David kilian.david@tum.de Room N5301