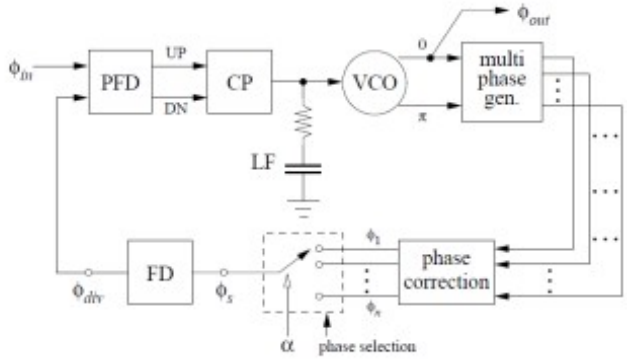
**Lehrstuhl für Schaltungsentwurf**
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

# High Bandwidth Fractional PLL using Phase Switching

*Masterthesis*




***Motivation:***

Fractional PLLs normally have relatively low bandwidths to avoid reference spurs. The reason for this is that the average frequency is achieved by switching between whole numbered dividers.
In this masterthesis this approach should be explored to keep reference spurs low and maintain a high PLL bandwdith to cut VCO noise.
This idea should be realised in an optimal fashion based on the modelling. An example circuit should be designed using a design environment for integrated circuits (Cadence).

***What needs to be done?***

- Develope an understanding of the fractional Phase Locked Loop
- Modelling of the fractional concept
- Circuit Design
- Possibly Layout

***What are good prerequesties for this work?***

- Basic understanding of clocked circuits
- Basic knowledge of circuit design
- Intrest in circuit design & modelling

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| Become curious? | → Contact: | Markus Dietl,<br>markus3.dietl@tum.de<br>Room N5303 |