Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Scientific Seminar on Structure, Architecture, and Application of Sensor Circuits

Chair of Circuit Design

Winter Semester 2025/2026

What you will learn in this seminar …

- At least 50% of this seminar is about the soft skills you need to become a successful engineer in science, but also in industry
- You will learn to:
  - Research state-of-the-art for a newly defined problem, and get a deeper understanding of the problem
  - Formulate a plan for solving the problem
  - Present technical work in a scientific paper, such that others can understand the content but also the motivation for the topic, what others have done in the field already, what you did new and better than others, as well as the remaining challenges after your work
  - Orally present the same topic to a group with the same intention

… **good work is often only recognized if it is also well presented (and for this, first of all,** it needs to be understood by others in a short time frame)!

Outline – Kick-Off Meeting

Today …

- Your work and duties during this seminar
- Timing & Deadlines: Submissions and presentations
- Grading of your work
- Presentation of topics by supervisors
- Selection of one topic per student
- Lecture: How to do literature research

Outline – Course of the seminar

- Then …
  - Lecture 2: How to write an article
  - Lecture 3: How to do a presentation
  - Work on your own: Text / Internet search / discussions
  - In case you need help: please contact your supervisor in advance and try to use your and his/her time efficiently
  - Take advantage of the supervisor's feedback, this is where you can learn most!
  - Show your results: report (4 pages) and oral presentation (12+3 min.)

Your work and duties

- Choose one of the topics
- Do research about the topic
- Write a scientific paper about the topic (4 pages)
- Prepare and give a scientific presentation (12 min + 3 min Q&A, this is the standard for conferences)
- For paper and presentation:
  - focus on basics of the problem and specific implementation
  - a template will be provided on Moodle

Your work and duties

1. Do a literature search and discuss your research results with your supervisor
2. Then study the literature
3. Develop an outline (content) for your paper and presentation
4. Discuss your outline with your supervisor (by appointment)
5. Work out the outline in your paper
6. Submit your paper
7. Summarize your results in a presentation
8. Submit the presentation

Grading

- ✓ Regular discussions (online/in presence) with the assigned supervisor about the progress of the work and the procedure
- ✓ Oral presentation of the results (12 min.) with subsequent discussion (3 min.) (50%)
- ✓ Scientific paper in IEEE style (4 pages): written elaboration of the results (50%)

Timing & Deadlines

	When?	What?
Kick-off	15.10.2025 14:00-15:30	Introduction & How to do a literature research **Participation is mandatory!**
Lecture 1	29.10.2025 17:00-18:30	How to write a scientific article
Lecture 2	14.01.2026 17:00-18:30	How to prepare and hold a presentation
Paper submission deadline	03.02.2026 (Tuesday) until 23:59 PM	In Moodle and via email to your supervisor
Presentations	05.02.2026, 10:00-17:00 Detailed schedule will follow	

Topics (Overview)

Topic	Supervisor	Available
	Kilian David	
Low Power PLL	Markus Dietl	
Time scales in spiking neuron circuits	Ferdinand Pscheidl	
Wide Input Range CD-Converter: A State-of-the-Art Survey	Tobias Chlan	
Topologies for in Hardware-Implemented Spiking Neural Networks and their Applications	Nikan Dehghan-Manschadi	
Ultrasound Transmit Sequences and Matched Filters	Leon Dixius	
Audio DAC *State-of-the-Art Techniques*	Moritz Gruber	
Voltage Regulator Design for Againsting Power Analysis Attacks	Pengcheng Xu	
Impact of Power Supply on AFEs & AI Accelerator	Pengcheng Xu	

LAST UPDATED 24.09.2025

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Time scales in spiking neuron circuits

and Spiking Neural Networks (SNNs)

Problem:
The direct interaction of Spiking Neural Networks (SNN) with the real world might require the simultaneous processing of information on very different time scales.

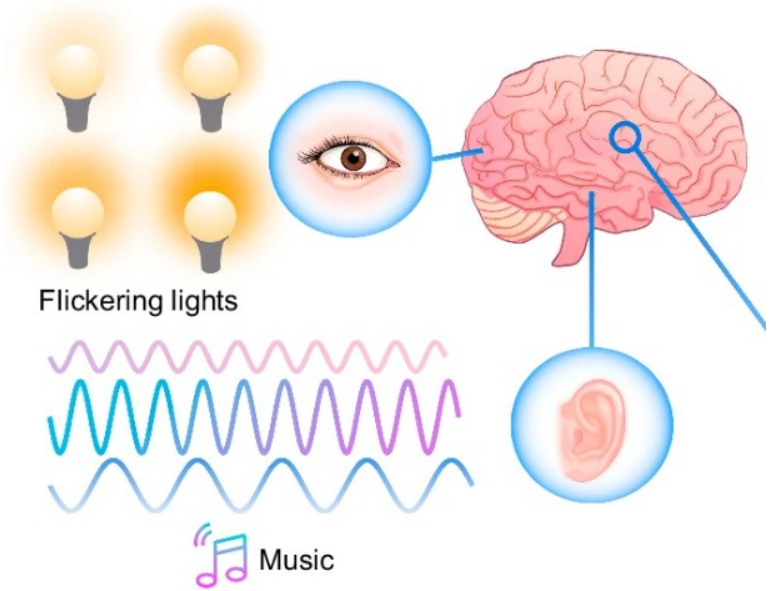

Figure 1. Tasks on different time-scales.

Focus:

- What defines the time scale on which single silicon neurons or synapses can process information?
- What time scales can be implemented with which approaches?
- How can networks of neurons be used to increase the time scale on which information can be processed?

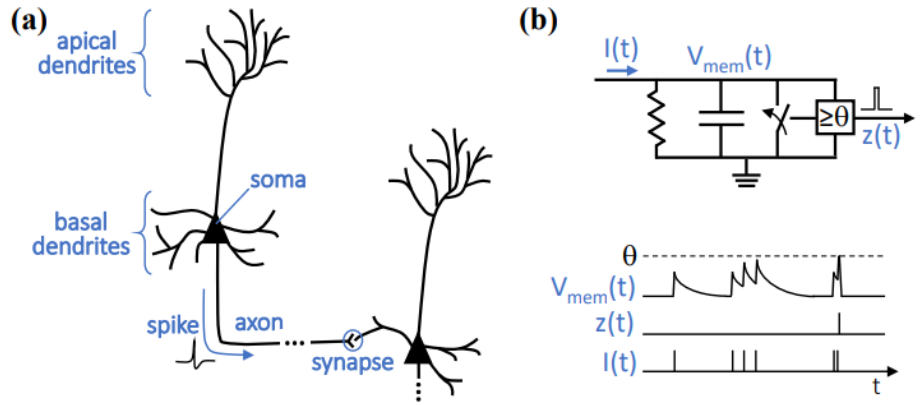

Figure 2. Spiking neuron dynamics.

Source Figure 1: https://doi.org/10.48550/arXiv.2106.01288
Source Figure 2: https://doi.org/10.1038/s41467-025-62251-6

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Wide Input Range CD-Converter: A State-of-the-Art Survey

State-of-the-Art, Design, Features, Comparison

Problem:
Need for efficient capacitance to digit converter considering topology, effort and efficiency (area, noise, current, resolution)

Focus

- State-of-the-Art: CD-Converters
  - Topologies: Delta-Sigma, SAR, Dual-Slope
  - Conversion concept? Is it directly Cap to Digit?
  - Efficiency (FoM), Resolution, …
  - Limitations of topology
- Comparison of topologies
  - Advantages/Disadvantages
  - Highlighting of the crucial trade-offs
  - Comparison table

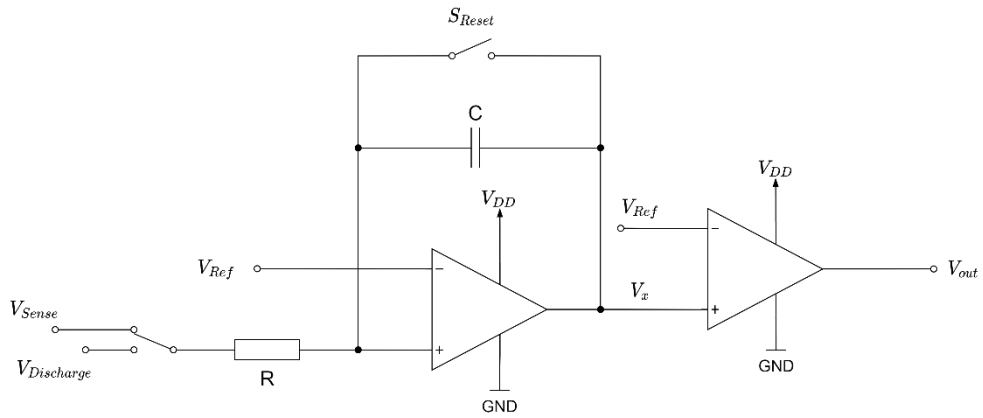

Figure 1. Dual-Slope Converter

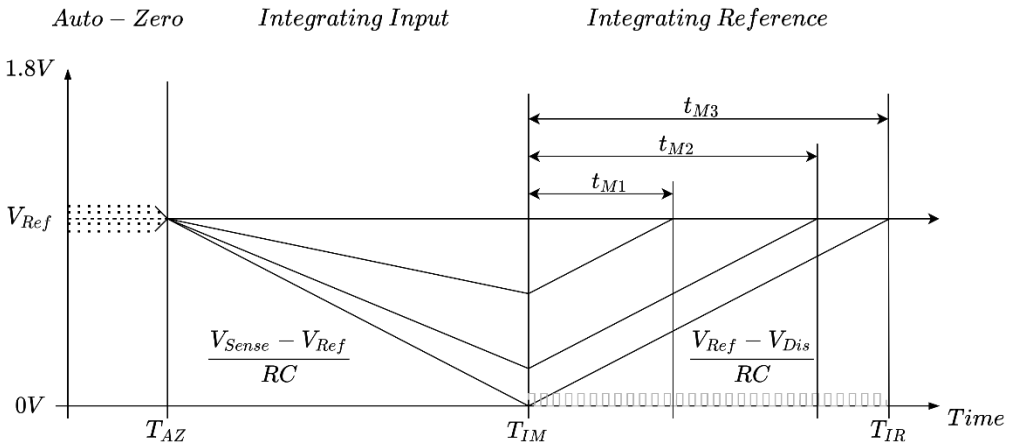

Figure 2. Typical dual-slope conversion cycle

Source Figure 1, 2: Analog-to-digital converter for the genration of keys with mechanical stress compensation, Tobias Chlan

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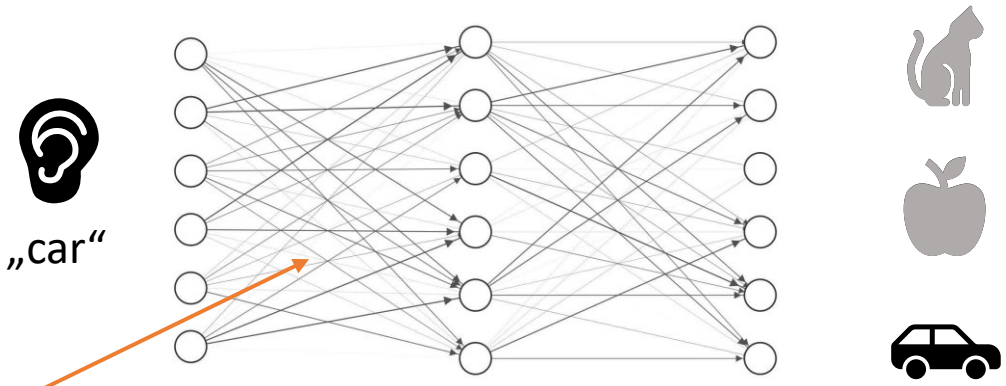
Topologies for in Hardware-Implemented Spiking Neural Networks and their Applications

Background:

- Spiking Neural Networks (SNN) are biological inspired Neural Networks that want to mimic the brain
- They use short electrical pulses, called „spikes“, to propagate information
- We can emulate and train them but „physical implementations“ with electronics are rare

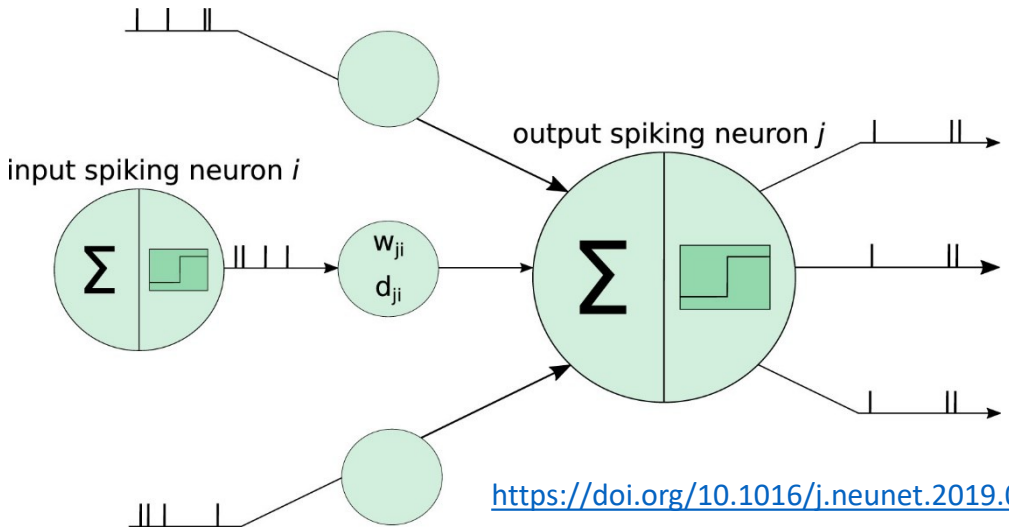
Goals:

- Understanding of SNNs and the hardware realizations of its components
- Researching different topologies/SNN-structures and their specific use case
- Compare different approaches and highlight challenges



https://www.baeldung.com/cs/spiking-neural-networks

Optimized Structure?



https://doi.org/10.1016/j.neunet.2019.09.004

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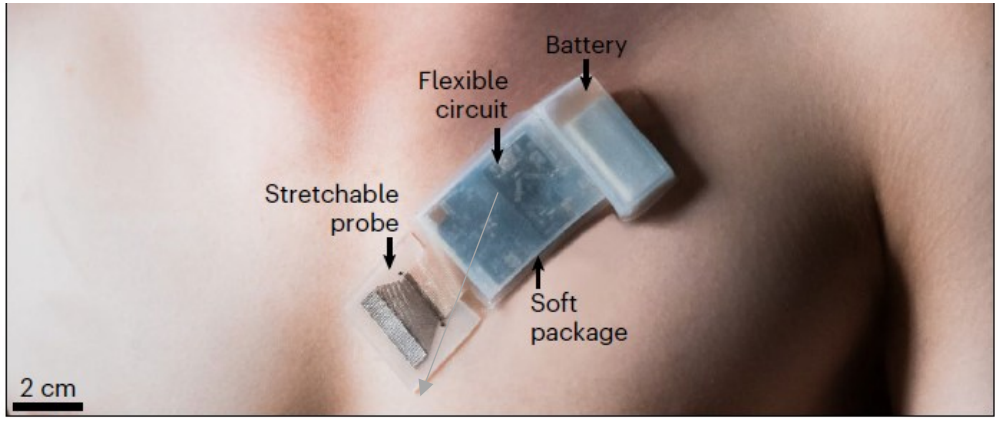
Ultrasound Transmit Sequences and Matched Filters

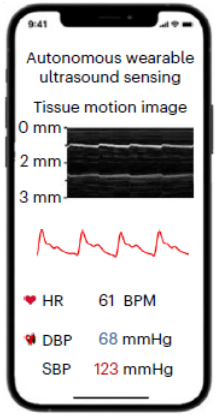
Working Principle Summary and SOA Analysis

Common ultrasound probes are bulky and wired to large control systems, which limits their usage to centralized facilities. A wearable ultrasound system could enable many new applications such as continuous cardiovascular monitoring [1] or advanced prosthetics control [2]. In ultrasound matched filters enable lower peak transmit voltages which could be beneficial for wearable applications.



In this topic, you are expected to:

- Investigate the different transmit sequenz / matched filter approaches and summarize their working principle.
- Categorize them in the context of low-power, wearable, integrated ultrasound.
- Analysis the advantage and limitation of the state-of-art works.



[1] Lin, M., Zhang, et.al., 2024. A fully integrated wearable ultrasound system to monitor deep tissues in moving subjects. *Nature Biotechnology*, *42*(3), pp.448-457.
[2] Yin, Zongtian, et.al., 2022. A Wearable Ultrasound Interface for Prosthetic Hand Control. *IEEE JBHI, 26(11), pp.* 5384 - 5393

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Audio DAC

State-of-the-Art Techniques

Background:
The human ear is remarkably good at perceiving audio signals across a wide dynamic range and detecting even the slightest distortions. Therefore, generating “good” quality audio imposes strict requirements on the dynamic range and total harmonic distortion (THD+N) of audio DACs.

Tasks:

- Understand the requirements for audio DACs
- Compare State-of-the-Art circuits:
  - Find different topologies and techniques: e.g. Delta-Sigma DACs, Digital PWM Class D Amplifiers, …
  - Compare topologies and find tradeoffs (power consumption, frequency, …)

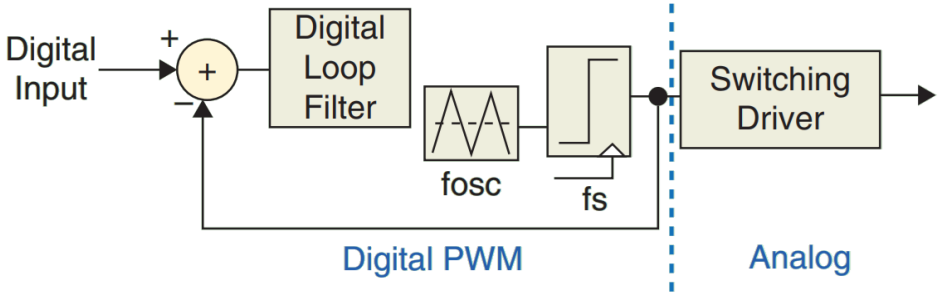

Figure 1. Example block diagram of a digital PWM class D audio amplifier.

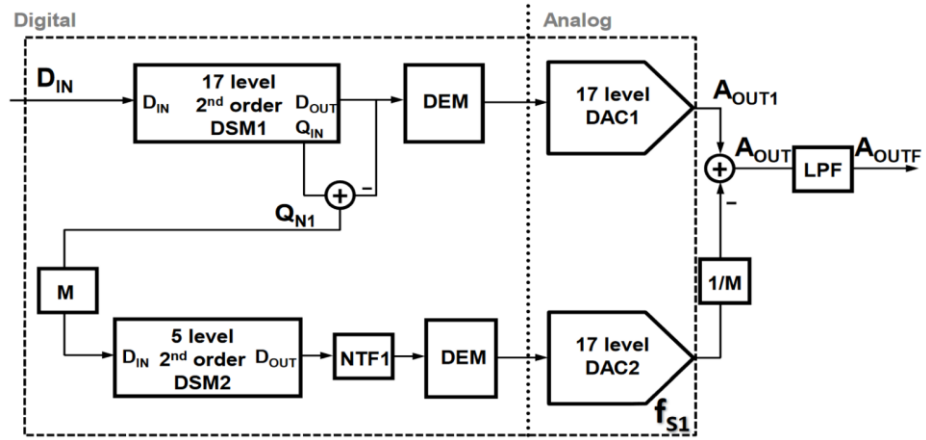

Figure 2. Example circuit of block diagram of a delta-sigma audio DAC.

Source Figure 1: X. Jiang, "Fundamentals of Audio Class D Amplifier Design: A Review of Schemes and Architectures," in IEEE Solid-State Circuits Magazine, vol. 9, no. 3, pp. 14-25, Summer 2017
Source Figure 2: M. G. Kim et al., "A stereo 110 dB multi-rate audio ΔΣ DAC with Class-G headphone driver," Proceedings of the IEEE 2014 Custom Integrated Circuits Conference, San Jose, CA, USA, 2014

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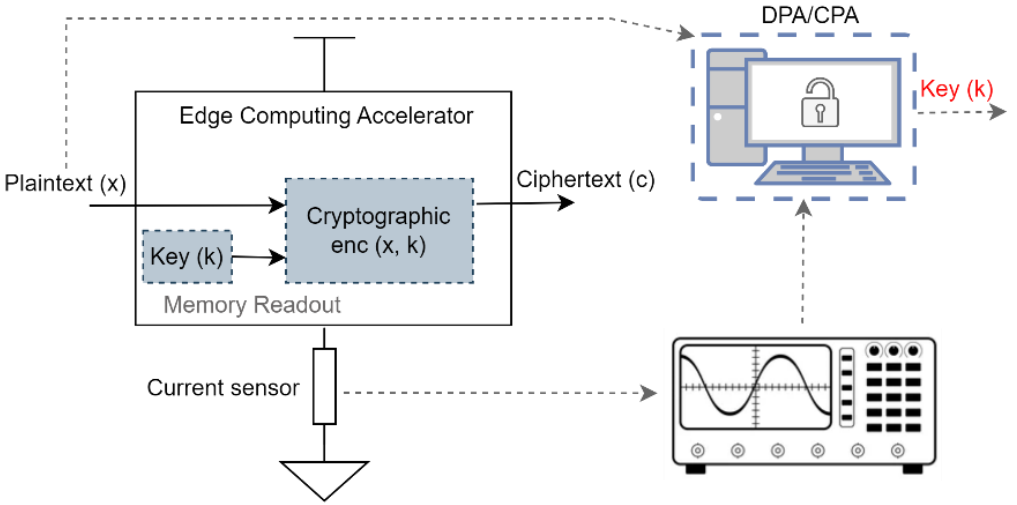
Voltage Regulator Design for Againsting Power Analysis Attacks

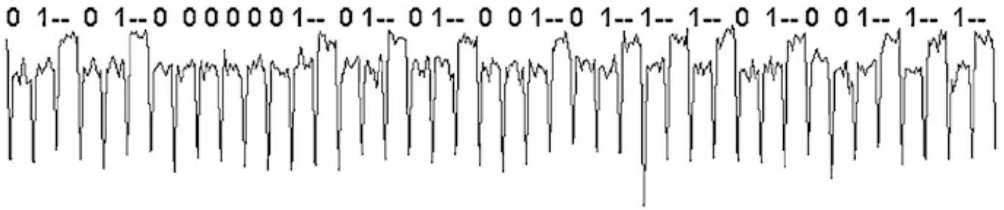
Design Principal Analysis and SOA Summary

In power-based side-channel attacks, an adversary observes the power current or voltage variations during the device's operation. In CMOS technology, the power consumption correlates with the activities being carried out by the device. Specifically, the energy usage of a circuit fluctuates depending on the actions of individual transistors. This relationship has revealed that the power consumption of an IC serves as a side channel, inadvertently exposing details about the internal operations, processed data, and activities occurring within the IC.



In this topic, you are expected to

- Summary and analysis the working principle of power analysis attacks (PAA) and the SOA work on voltage regulator design to against PAA.
- Summary and analysis the new feasure of PAA in edge devices.
- Summary the side channel analysis (SCA) attacks resistance measurement solutions and how SCA attacks resistance is measured from a voltage regulatro design.



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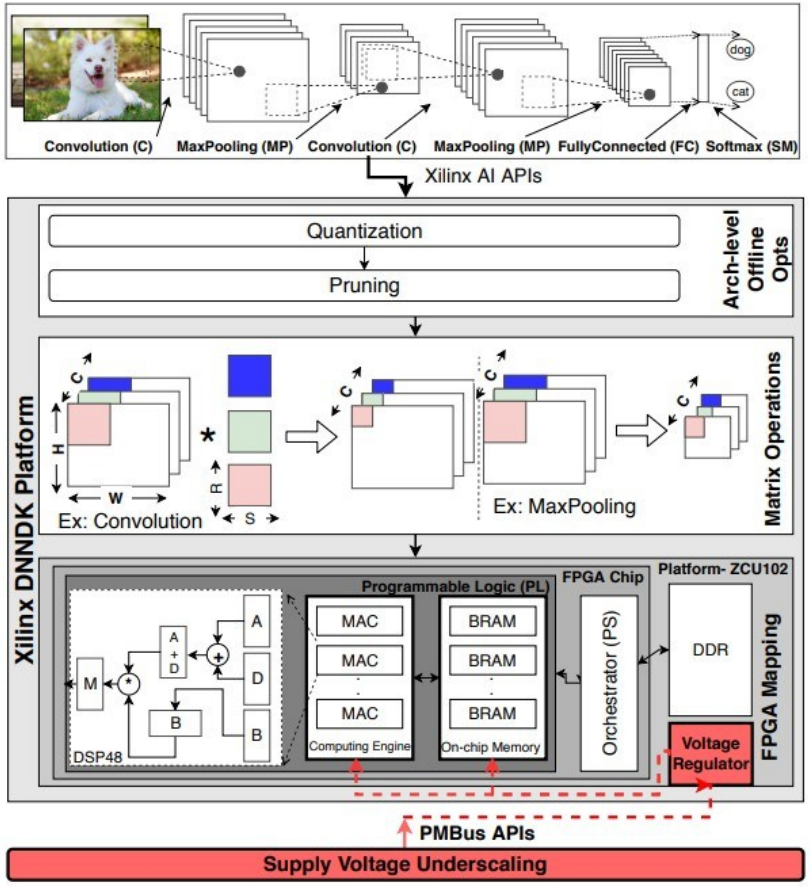
Impact of Power Supply on AFEs & AI Accelerator

Design Principal Analysis and SOA Summary

In edge systems, tight energy budgets force converters to use burst/PFM modes and aggressive duty-cycling. The resulting supply ripple, droops, and jitter propagate into the analog front end (AFE) and on-chip inference: bias and timing shift in op-amps/ADCs, event thresholds misfire in LC-ADC/SNN, and digital accelerators suffer timing/bit errors under undervolting. Classic mitigation is high PSRR, but this costs energy and area. Recent work explores hardware-aware training, digital post-correction, and co-design—yet a unified, task-level view is still emerging.

In this topic, you are expected to:

- Summarize & analyze the mechanism from VDD noise/ripple/drop.
- Review the state of the art: the impact of power supply on digital ANN accelerators, Analog AFEs, SNN / neuromorphic & event-driven AFEs, Mixed-signal/IMC and corresponding technique to compensate this impact from power supply.



B. Salami et al., "An Experimental Study of Reduced-Voltage Operation in Modern FPGAs for CNN Acceleration," DSN 2020.