

Ultra-Low-Power Bandgap Reference Circuit Design

Introduction

Ultra-low-power bandgap reference (BGR) circuits are key building blocks in power management ICs, sensor interfaces and always-on systems. In this topic, you will work on the design of a CMOS bandgap reference with very low power consumption while maintaining good line sensitivity, temperature stability and process robustness.

- Circuit architecture exploration for ultra-low-power BGR,
- Transistor-level CMOS circuit design and simulation,
- Layout implementation with matching-aware design,
- Post-layout extraction and post-layout simulation,
- Performance analysis across process, voltage and temperature (PVT) corners.

We already have sufficient background material and design flow support for you to start smoothly.

Workflow

The following workflow is expected in your work:

- Literature Review: Read state-of-the-art (SOA) papers on ultra-low-power bandgap reference circuits. Analyze and summarize the key design techniques and corresponding trade-offs.
- Define Specifications: Based on target applications, define the circuit architecture and design specifications. Analyze the circuit and summarize the verification/simulation checklist and target performance metrics.
- Circuit Design: Design and simulate the circuit using Cadence analog design tools in CMOS technology. The work includes schematic design, pre-layout simulation, layout, parasitic extraction and post-layout verification.

Requirement

- Strong background in CMOS analog integrated circuit design.
- Experience with Cadence analog design tools is preferred.
- Good self-learning ability and motivation for independent research work.

Reference

- Design of Analog CMOS Integrated Circuits, Behzad Razavi
- CMOS Voltage References: An Analytical and Practical Perspective, Gabriel Alfonso Rincón-Mora

Contact

Dr. Pengcheng Xu

Email: pengcheng.xu@tum.de

TEL: +49 89 289 22908

