Lehrstuhl für Schaltungsentwurf
Fakultät für Elektrotechnik und Informationstechnik
Technische Universität München

Requirements of Ultra Fast Locking Low Power PLL

Masterthesis

.

Motivation:

In low power sensorsytems clocks are needed to clock the ADC. To save power only a low power 32kHz Xtal clock is continously running. The high frequency (20MHz-50MHz) clock is powered down for most of the time and only switched on for a short time.
In this thesis the requirements of the system´s clocking needs to be understood and a proposal of a solution should be developed.

What needs to be done?

- Develope an understanding of the Sensor System
- Modelling of Clocking
- Breaking down the requirements to blocklevel
- Development of solution at block level

What are good prerequisites for this work?

- Basic understanding of fourier transformation
- Basic knowledge of circuit design
- Intrest in modelling

Become curious?	→ Contact:	Markus Dietl, markus3.dietl@tum.de Room N5301