Active Body-Bias Linearization for Wide-Band GmC Based Continous-Time ΣΔ ADCs in 22 nm FD-SOI

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We present a linearization technique for differential transconductors in fully depleted silicon-on-insulator (FD-SOI) CMOS technology. Here, dynamic self-biasing is employed at the back-gate node, thereby the non-linearity of the main differential input pair is compensated. The method yields excellent linearity and is highly applicable in high-bandwidth and wide-swing GmC based continuous-time Sigma-Delta modulators (CT-SDMs). Predominantly, the CT-SDMs loop filters are realized by operational amplifiers (opamp) with active-RC feedback. This yields high linearity due to the virtual ground node at the opamps input. However, this comes at a cost of power efficiency as the preceding stages need to be capable of driving the relatively low-impedance RC input. GmC topologies overcome this limitation by offering fully capacitive, and hence high input impedance. However, linearity is impaired due the full signal excitation at the input. Recently, various approaches mitigating this impairment have been shown [1-3]. Here, the proposed technique overcomes this by active linearization of the input G_m cell. Transistor level simulations show linearity improvements of 25 dB while only increasing the loop filters power dissipation by 10 %. Process corner, voltage, temperature (PVT) as well as mismatch dependency is evaluated proving the concepts robustness and efficiency. [4]

The concept is is made possible by utilizing FD-SOI CMOS technology. Recently, various techniques exploiting the technology feature of an increased body-bias voltage V_BB range have been reported [5], [6]. Contrary to bulk CMOS, in FD-SOI the body node is isolated by a fully depleted insulation layer and hence does not form a reverse bulk-source diode, allowing to freely choose the bulk voltage.

Here, transconductance $G_\mathrm{m}(V_\mathrm{in})$ is linearized by applying a negative feedback signal to the back-bias node, compensating the non-linearity of G_m. By carefully matching the gradients of each respective non-linear transfer function, $\mathrm{NL_F}$ for the front gate, $\mathrm{NL_B}$ for the back-gate, a linear overall transfer curve $G_\mathrm{m}(V_\mathrm{in})$ can be achieved. PVT robustness is provided by setting the gain A_B using a diode-load and by employing a replica input.

This linearization method is highly applicable for CT-SDMs and can be combined with other linearization schemes, as source degeneration or by using a voltage tracking GmVC. We prove the concept utilizing the GmVC architecture [7] in an exemplary 4 GHz third order CT-SDM with 250 MHz bandwidth and a SQNR of 79 dB. As shown on Fig. 3, the concepts here yields 25 dB improvement in third order intermodulation (IM3) products close to the bandwidth edge.

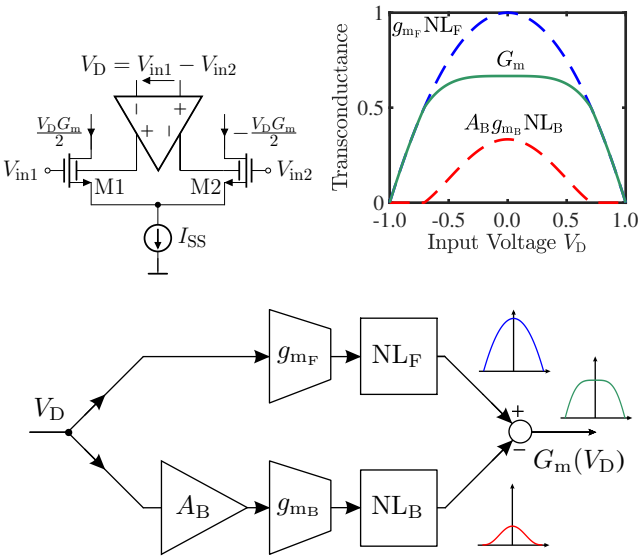

Fig. 1: MOS transconductor with active body bias linearization, its Block diagram representation, as well as Resulting G_m as front- and back-gate g_mF and g_mB. [4]

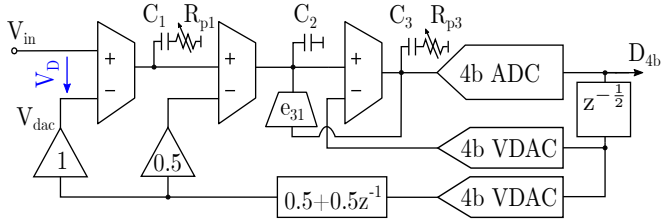

Fig. 2: Third order CT-SDM System architecture. [4]

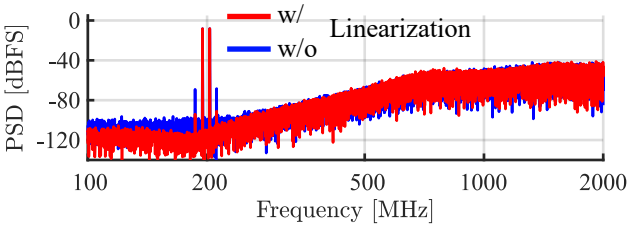

Fig. 3: Simulated power spectrum (65536 points). [4]

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