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High Resolution and High Sampling Rate Hybrid ADC for Electrically Modulated Magnetolectric Sensor

Abstract: The current development of thin film magnetolectric (ME) sensors ensures that ME technology is becoming a prospective candidate to read magnetic signals with ultra-low amplitude in the pT/\sqrt{Hz} regime. In principle, a read-out scheme-based electrically modulated ME sensor requires high bits resolution in the Analog-to-Digital converters (ADC) with up to 20 bits or higher. It is important to understand the noise limitations to quantify the minimum detectable signal and sampling frequencies for optimal measurements and reconstruct the magnetic input signal. The main obstacle for read-out schemes is the need for extremely low noise floors at the final sensor system output and how high-precision ADC is limited at intermediate sampling frequencies.

The main aim of this proof of concept is to evaluate a hybrid ADC for an Electrically Modulated ME sensor. This kind of sensor works at a resonance frequency of 510 kHz with a modulation amplitude response of depth as lowest as 0.01% for low magnetic input signals. The dynamic range of the sensor is 98 dB and because of the Limit-of-Quantification (LOQ), this implies a requirement of a Signal-to-Noise Ratio (SNR) of 118 dB. This means, it is required an ADC with an effective number of bits (ENOB) of 19.3 bits with a sampling frequency of at least 1.25 MHz.

The ME (*converse magnetolectric thin film sensor*) modulation characteristics have been simulated in a Cadence environment to evaluate the ADC proof of concept. A magnetic input signal of 1 nT is equivalent to 0.06% of the depth modulation index used for evaluation analysis. The structure of the proposed hybrid ADC is

presented in Fig.1. It works as follows: in the first stage, coarse ADC makes a first approximation, the residuo is amplified to give a full-scale range to the fine ADC. With this full-scale input, the quantization noise of the second ADC is reduced, and finally, the digital correction achieves a resolution of 20 bits and an 8 MHz sampling rate. The concept has been modelled in Verilog-A, and simulation results will be presented.

Finally, an outlook on future hybrid ADC perspectives and challenges, especially for ME sensors will be presented. For further optimizations this ADC concept will be integrated into an ASIC (*application-specific integrated circuit*).

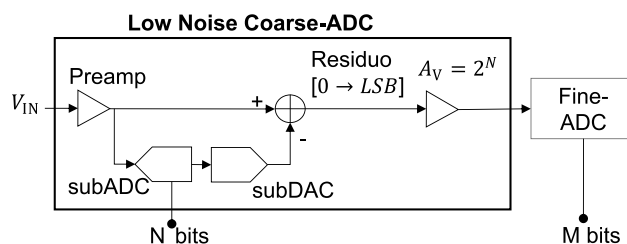


Fig. 1: Block Diagram of a proposed Hybrid ADC for high resolution ($N = 4.5 \text{ bits} + M = 15.5 \text{ bits}$) and 8 MHz sampling rate.

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References

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