Ultra-Low Frequency Digital Controlled Oscillator using CMOS Thyristor Based Delay Elements

MD Wasif Absar, Anton Gelaeschus, Julian Singer, Andreas Bahr

Institute for Integrated Circuits, Technical University of Hamburg
Email: anton.gelaeschus@tuhh.de

Abstract

Optogenetics has paved ways for a new group of optoelectronic controlled neural implants to address disabilities and genetic disorders even in complicated neural networks of vertebrates. Most of these systems use Laser or µLEDs to trigger the genetically modified photosensitive brain regions. Maintaining the luminance of the light source for a definite duration to produce the desired effect without heating up the localized portion of the brain is critical for such implants. Generally, pulse width modulators are used to create the electrical pulses that eventually control the optical source. The frequency of the signals generated by the modulator should be in correspondence with the biological signal frequency and the kinetics of the photosensitive proteins that lies in the range of 20 - 200 Hz. In an advent to pursue lower frequency generation, thyristor based oscillators were studied and a novel thyristor based digital controlled oscillator (DCO) is proposed in this work. A handful of research articles resorted to a frequency tuning scheme where each fundamental thyristor block acts as a half circuit to delay either the positive or negative edge of the clock. Changeable time delays can also be produced with variable oscillator stages and controlling those stages with the help of multiplexers. This work attempted to simplify the overall design by just using the basic thyristor block and integrate the bit control within the fundamental block to save die area and power. The modified thyristor block when used to implement a three stage DCO gives out a tuning range of approximately 28 Hz. Efforts have been made to enhance this tuning range by incorporating variable stages and later variable capacitive loading was proposed for a seamless tuning operation. The final design shows a wider tuning range of 166.18 Hz starting from a low frequency value of 28.78 Hz to a maximum range of 194.96 Hz. Device dimensions obtained through a set of parametric analysis gave out reasonable sized devices for higher area efficiency. Simulation results of a three stage thyristor based DCO for different bit combinations show an average power consumption of 500 - 600 pW approximately. All the designs were characterized using SPICE simulations in Cadence Analog Design Environment at 180nm CMOS Technology.