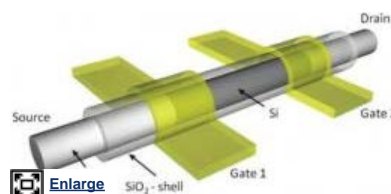


Universal transistor serves as a basis to perform any logic function

December 20, 2011 by Lisa Zyga feature



The reconfigurable transistor's core consists of a nanowire structure embedded in a silicon dioxide shell. Electrons or holes flow from the source at one end of the nanowire through two gates to the drain at the other end of the nanowire. One gate is used to program the p- or n-polarity, whereas the other gate tunes the conductance through the

nanowire. Image credit: ©Nanlab gGmbH

(PhysOrg.com) -- Most of today's electronics devices contain two different types of field-effect transistors (FETs): n-type (which use electrons as the charge carrier) and p-type (which use holes). Generally, a transistor can only be one type or the other, but not both. Now in a new study, researchers have designed a transistor that can reconfigure itself as either n-type or p-type when programmed by an electric signal. A set of these "universal transistors" can, in principle, perform any Boolean logic operation, meaning circuits could perform the same number of logic functions with fewer transistors. This advantage could lead to more compact hardware and novel circuit designs.

The researchers who designed the transistor, led by Walter M. Weber at Nanlab gGmbH in Dresden, Germany, have published the new concept in a recent issue of *Nano Letters*.

"Synthetic nanowires are used to realize the proof-of-principle," Weber told *PhysOrg.com*. "However, the concept is fully transferable to state-of-the-art CMOS silicon technology and can make use of self-aligned processes."

The new transistor's core consists of a single nanowire made of a metal-semiconductor-metal structure, which is embedded in a silicon dioxide shell. Electrons or [holes](#) flow from the source at one end of the nanowire through two gates to the drain at the other end of the nanowire. The two [gates](#) control the flow of electrons or holes in different ways. One gate selects the transistor type by choosing to use either electrons or holes, while the other gate controls the electrons or holes by tuning the nanowire's conductance.

Using a gate to select p- or n-type configuration is quite different from conventional [transistors](#). In conventional transistors, p- or n-type operation results from doping that occurs during the fabrication process, and cannot be changed once the transistor is made. In contrast, the reconfigurable transistor doesn't use any doping. Instead, an external voltage applied to one gate can reconfigure the transistor type even during operation. The voltage causes the Schottky junction near the gate to block either electrons or holes from flowing through the device. So if [electrons](#) are blocked, holes can flow and the transistor is p-type. By applying a slightly different voltage, the reconfiguration can be switched again, without interfering with the flow.

The scientists explain that the key to making this reconfiguration work is the ability to tune the electronic transport across each of the two junctions (one per gate) separately. Their simulations showed that the current is dominated by tunneling, suggesting that the nanowire geometry plays an important role in the ability for independent junction control.

Because the reconfigurable transistor can perform the logic functions of both p- and n-type FETs, a single transistor could replace both a p- and n-type FET in a circuit, which would significantly reduce the size of the circuit without reducing functionality. Even at this early stage, the reconfigurable transistor shows very good electrical characteristics, including a record on/off ratio and reduced leakage current compared to conventional nanowire FETs. In the future, the researchers plan to further improve the transistor's performance.











"We are varying the material combinations to further boost device

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





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performance,” Weber said. “Further on, first circuits implementing these devices are being built. ... The biggest challenge will be to incorporate the extra gate signals in the cell layout allowing flexible interconnection to the other transistors.”

More information: André Heinzig, et al. “Reconfigurable Silicon Nanowire Transistors.” *Nano Letters*. DOI: [10.1021/nl203094h](https://doi.org/10.1021/nl203094h)

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[Pattern_chaser](#)
Dec 20, 2011

If this comes to fruition (real-world devices), it could be incredible!

Rank: **not rated yet**

[Corban](#)
Dec 20, 2011

Smaller, cooler, better, faster. This is daft!

Rank: **5 / 5 (1)**

[rawa1](#)
Dec 20, 2011

This transistor is apparently smarter, than most of posters here...

Rank: **2.1 / 5 (7)**

[antialias_physorg](#)
Dec 20, 2011

“ The biggest challenge will be to incorporate the extra gate signals in the cell layout allowing flexible interconnection to the other transistors.

Rank: **5 / 5 (4)**

This just screams for a multi-layer layout.

The challenge will be to get these nanowires to either deposit or grow in situ at a high quality and regularity for integrated circuits.

Since it only uses SiO2 and not expensive monocrystalline Si this could be a real game changer.

Exciting stuff.

[Eikka](#)
Dec 20, 2011

How do they overcome the problem, that the charge carriers in a p-type transistor are less mobile than in the n-type?

Rank: **3.7 / 5 (3)**

In a complementary device, the p-type transistor has to be physically 2..3 times bigger than the n-type transistor to get the operating point right. Matching the transistors sets the "tipping point" of the circuit where it changes logical state, and when evenly matched, the tipping point should be half the driving voltage to give the maximum tolerance for errors.

This is the reason why NAND logic is preferred over NOR logic. Both gates can be used to perform any boolean logic function - they're "universal gates. They're mirrored versions of each other, but the requirement to match the p/n transistors makes NOR much bigger on silicon because of the lower conductance of the p-type transistor.

Perhaps they can limit the conductance of the n-type configuration somehow, but I suspect that increases the complexity of the control circuitry a great deal.

[PaulRC](#)
Dec 20, 2011

so, how long until some a.i. chips that reconfigure themselves to run algorithms more efficiently? amazing breakthrough, hope it markets sooner rather than later and is a good as they

Rank: **not rated yet**

advertise.

[Koen](#)
Dec 20, 2011

If you ask me, not even the math has developed to describe the logic implemented by these two-gates transistors.

Rank: **1 / 5 (2)**

[tpb](#)
Dec 20, 2011

More interesting to me is the possibility of a transistor that can switch AC signals without having to put two transistors in a series-opposed configuration.

Rank: **3.7 / 5 (3)**

There are some new switching power supply topologies that are 98% efficient from AC in to DC out that require a transistor that can switch either polarity on or off.

[twasnow](#)
Dec 20, 2011

So what is the package output going to look like G, D, S, and now C for Channel?

Rank: **5 / 5 (1)**

It could greatly increase the functionality of FPGA's, with a cpu you get to constantly read code so actual functionality isn't change, but with FPGA's it allows for essentially fully utilized segments, meaning for one much smaller pga's required, approximately 1/4 the size (because it means the ability eliminate all non-needed gates). It also means the ability to change the logic while live based on input.

Damn, I wonder if that's patented yet. (probably but I am going to do a search)

get this sort of thing in to an FPAA (field programmable analog array) and we may have a new contender for high level machine intelligence.

[twasnow](#)
Dec 20, 2011

tpb, I am not sure how you think a bi channeled fet is going to help you there. but maybe I just don't know what type of circuit you're talking about

Rank: **not rated yet**

(also 98% high efficiency switching power supplies have been around a long time) but that is DC-DC, not AC-DC in which you get an efficiency of 96% x 98% (AC-DC conversion eff. x voltage level eff.) meaning actually eff. is more like 94%)

[Eikka](#)
Dec 20, 2011

“ (also 98% high efficiency switching power supplies have been around a long time) but that is DC-DC, not AC-DC in which you get an efficiency of 96% x 98% (AC-DC conversion eff. x voltage level eff.) meaning actually eff. is more like 94%)

Rank: **not rated yet**

DC-DC conversion actually involves a DC-AC-DC conversion. There's no general rule how efficient it can be, because it depends on the topology, the parts, and the specific voltages and currents you need. All that can be accurately said is that it's going to be less than 100%.

[tpb](#)
Dec 20, 2011

There are some new resonant topologies that do PFC and output DC regulation directly off the AC line in a single stage so that you don't multiply the losses of two circuits as discussed by twasnow. The input bridge rectifier is also removed along with its losses. 2 volts / 120 = approx. 1.7%

Rank: **not rated yet**

[that_guy](#)
Dec 20, 2011

This may benefit FPGAs, but it will never hit your consumer computing needs.

Rank: **3.5 / 5 (2)**

To grow or place nanowires in very specific places is not exactly a cost effective strategy - New equipment, new setup, new methods, a high vector for defects, in addition to the expense of a non-lithographic layer...

Just saying, right now, anything that goes into the computer or phone has to be able to be applied lithographically, or an entirely new process altogether - instead of additive in addition

to lithography.

If you don't agree with me, show me your memristor chip.

Until then, we have to wait until intel finally pulls its deathgrip off of silicon, and converts over to graphene.

[twasnow](#)
Dec 20, 2011
actually that_guy, take a look at this
<http://ic.e.se.upe...2006.pdf>

Rank: **not rated yet**

although I don't think it is in production stage it is EXACTLY what is required for this.

[ShiftyOx88](#)
Dec 21, 2011
So I can see how this will make chips smaller, and possibly more effective(more processing == more effective), but wouldn't the ability to change this gate(the whole point) require more power?

"Instead, an external voltage applied to one gate can reconfigure the transistor type even during operation."

So now we must add an external voltage, to EACH gate, and then the control circuitry to actually know when and what state to change EACH gate into

[plasticpower](#)
Dec 21, 2011
@that_guy, I think you missed this bit:

Rank: **4 / 5 (1)**

"Synthetic nanowires are used to realize the proof-of-principle, Weber told PhysOrg.com. However, the concept is fully transferable to state-of-the-art CMOS silicon technolog"

So yes, it will show up in consumer tech. Very soon, actually.. I can't wait to play with an FPGA that's built on this technology!

[Tachyon8491](#)
Dec 21, 2011
Rank: **5 / 5 (1)**
Brilliant invention... I can see it working in great simplification of dedicated DSPs and FPAs. What concerns me is dynamic reconfiguration during operation in other applications - this adds the need for another (software) layer of control, and complicates program design, as also implying an unavoidable reduction in processing speed. An interesting parameter that is not quoted in the article is frequency response and cut-off frequency. Hope to see this technology develop more...

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