# A Perpendicular Spin Torque Switching based MRAM for the 28 nm Technology Node

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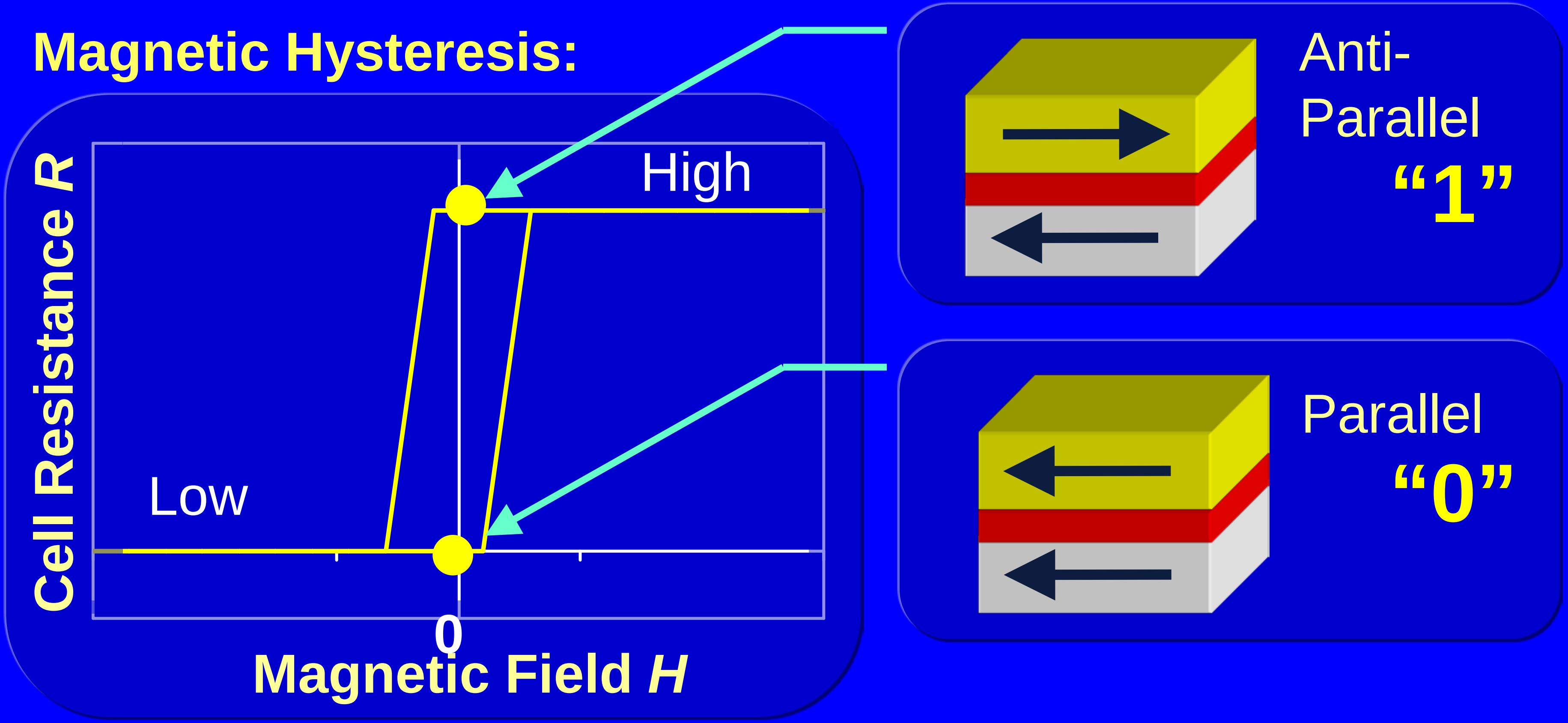
# Outline

- Perpendicular Spin Torque (P-ST) based MRAM
  - A New Concept
- Assessment for 28 nm Node
  - Data Retention
  - Low Switching Currents
  - Cell to Cell Interaction
  - Barrier Reliability
- Cell Layout
- Read Analysis

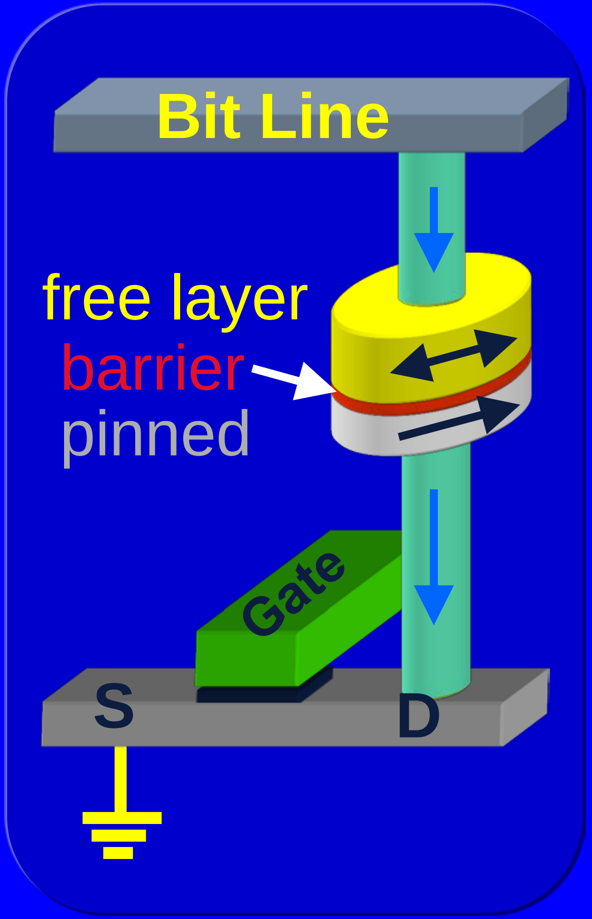
# Conventional MRAM

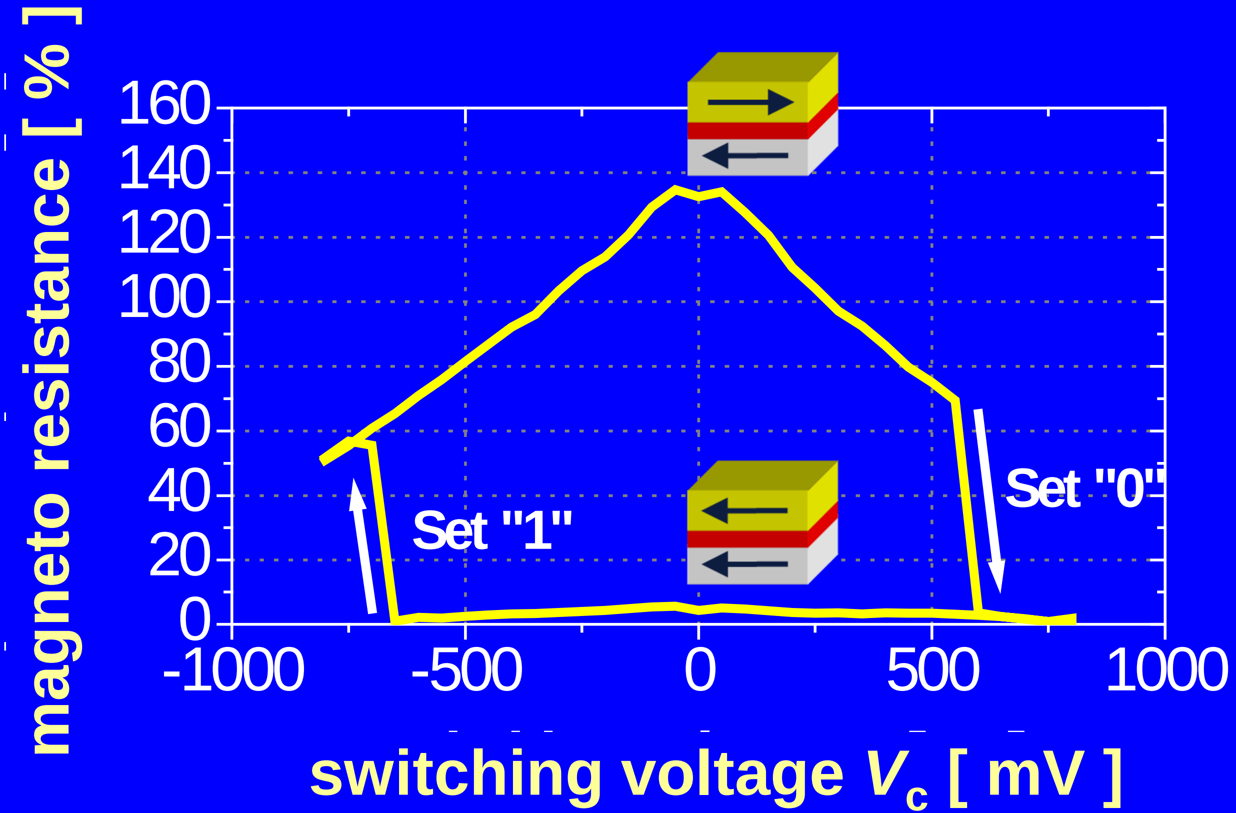
**Magnetic Hysteresis:**



- **WRITE:**
  **Word/Bit line field used to set magnetic free layer**
- **READ:**
  **Electrical determination of R by sense amplifiers**

# Spin Torque Select-Based MRAM



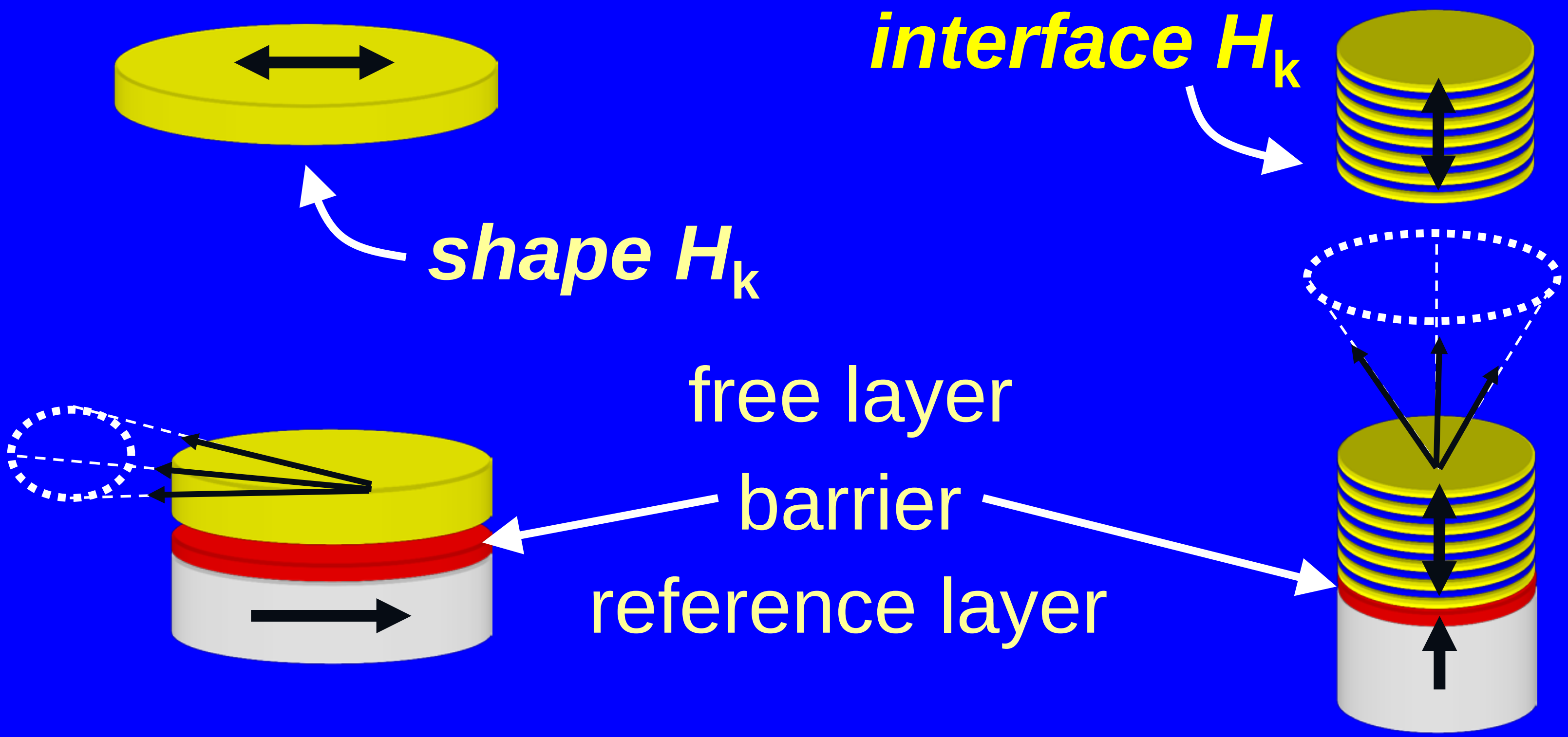


- ↳ Writing is done by a critical select current

# Perpendicular Anisotropy

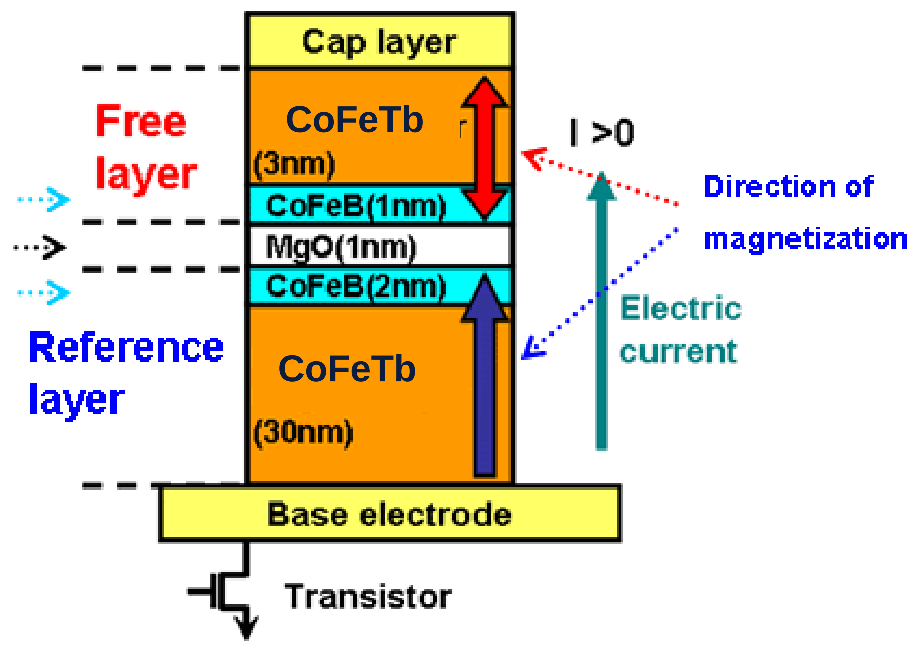
**In-Plane Magnetization**

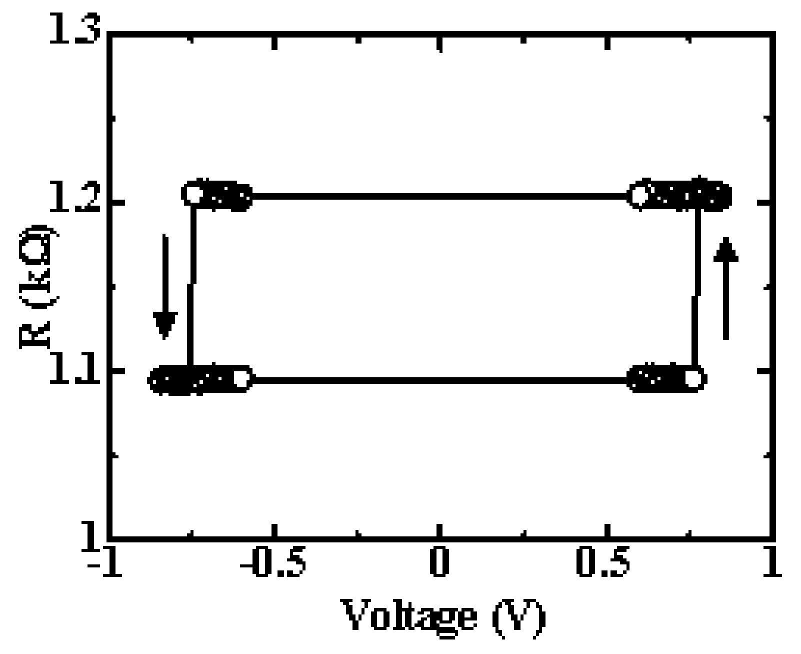
**Perpendicular Magnetization**



⇘ Perpendicular anisotropy is very high

# Realization



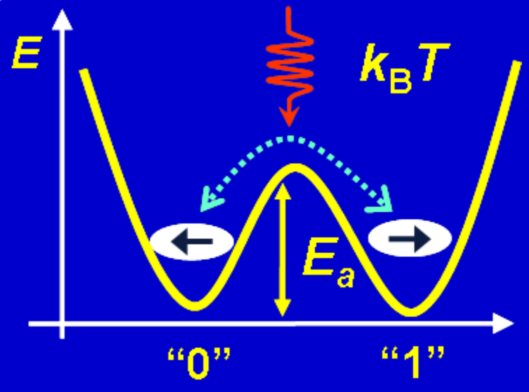


*Source: "Spin transfer switching in TbCoFe / CoFeB / MgO / CoFeB / TbCoFe magnetoresistive tunneling junctions with perpendicular magnetic anisotropy" , M. Nakayama et al. , BB-09, 52nd Magnetism and Magnetic Materials Conference (MMM) in Tampa, Nov. 2007*

↳ Feasibility of concept is demonstrated

↳ MTJ stack engineering is important

# Scalability of Activation Energy

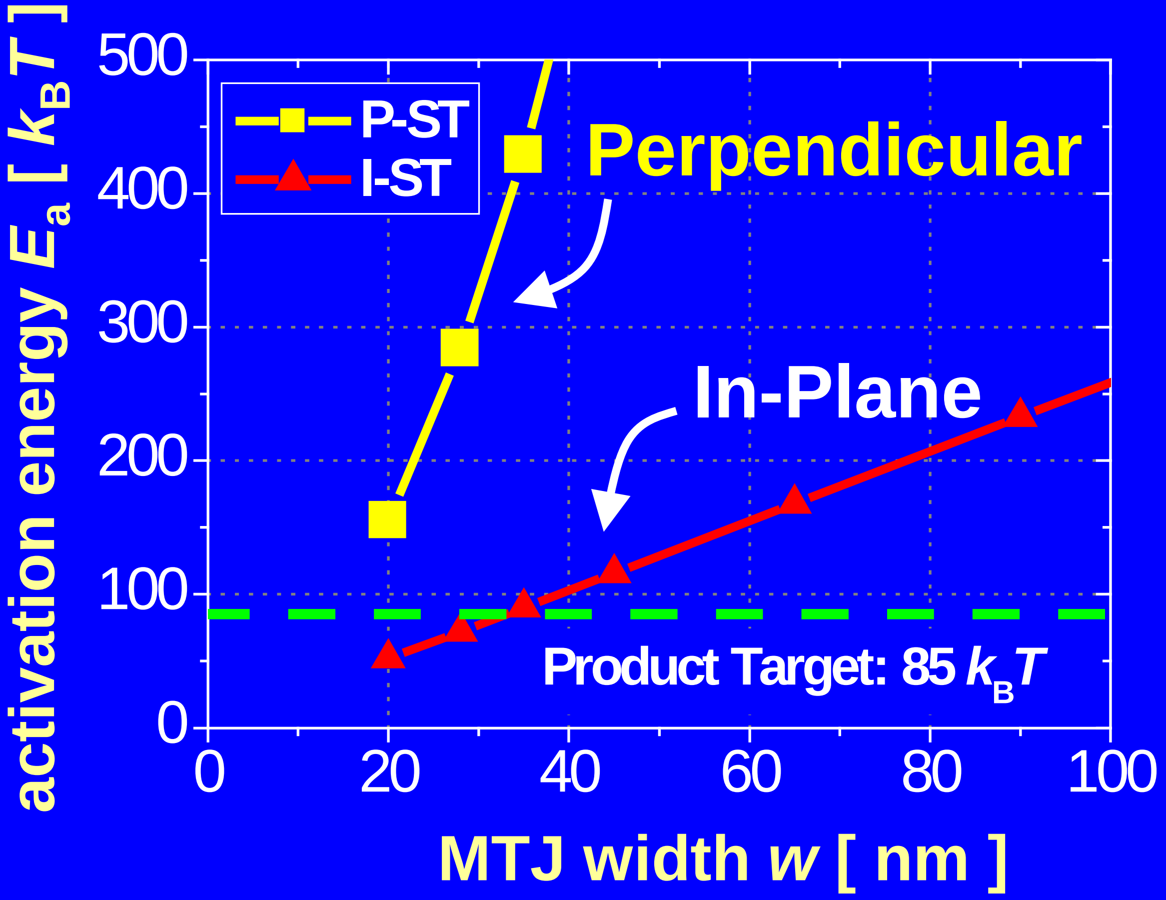


$$E_a = \frac{1}{2} Vol * M_s * H_k$$

MTJ size

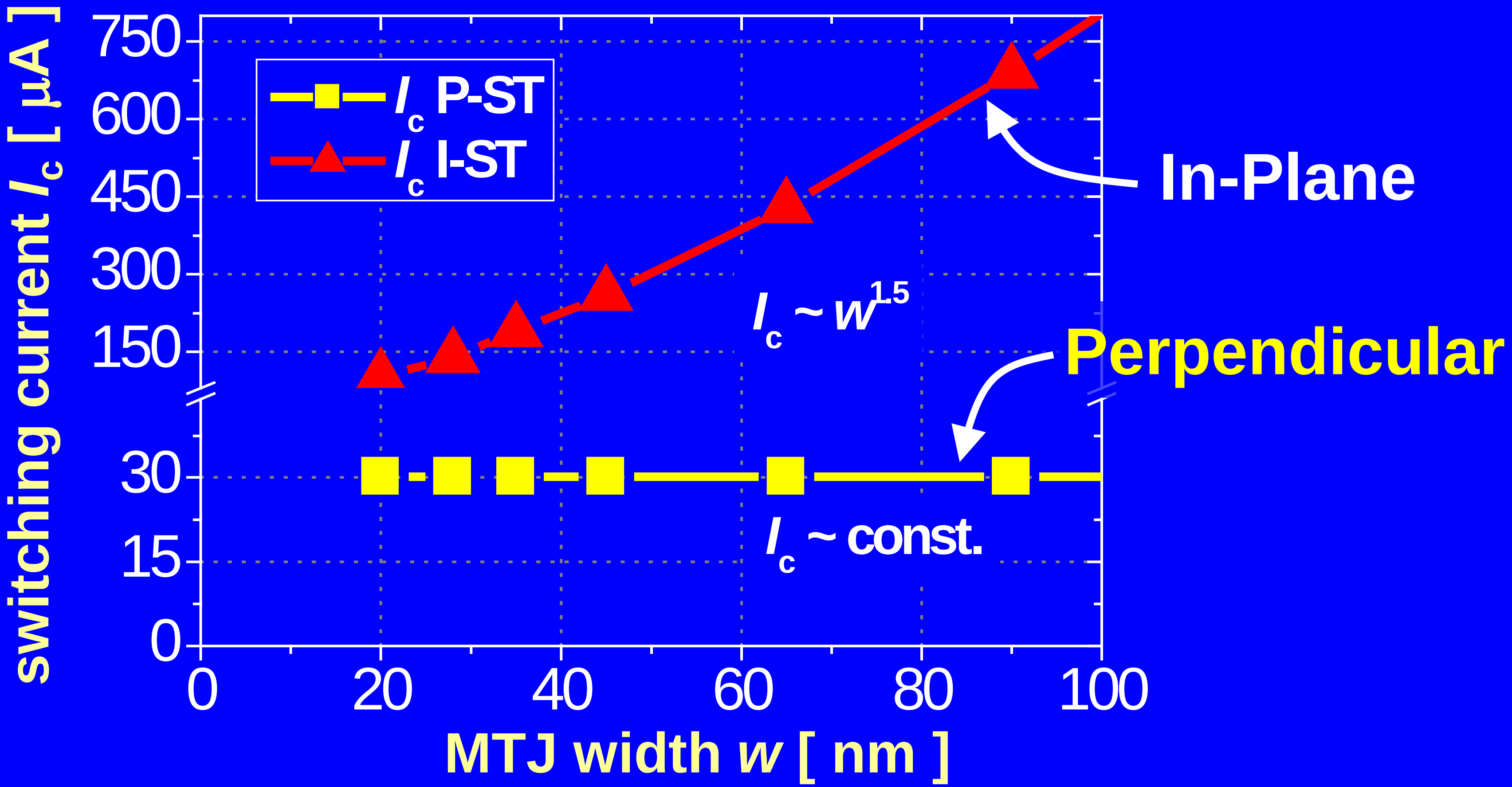
Material

Anisotropy



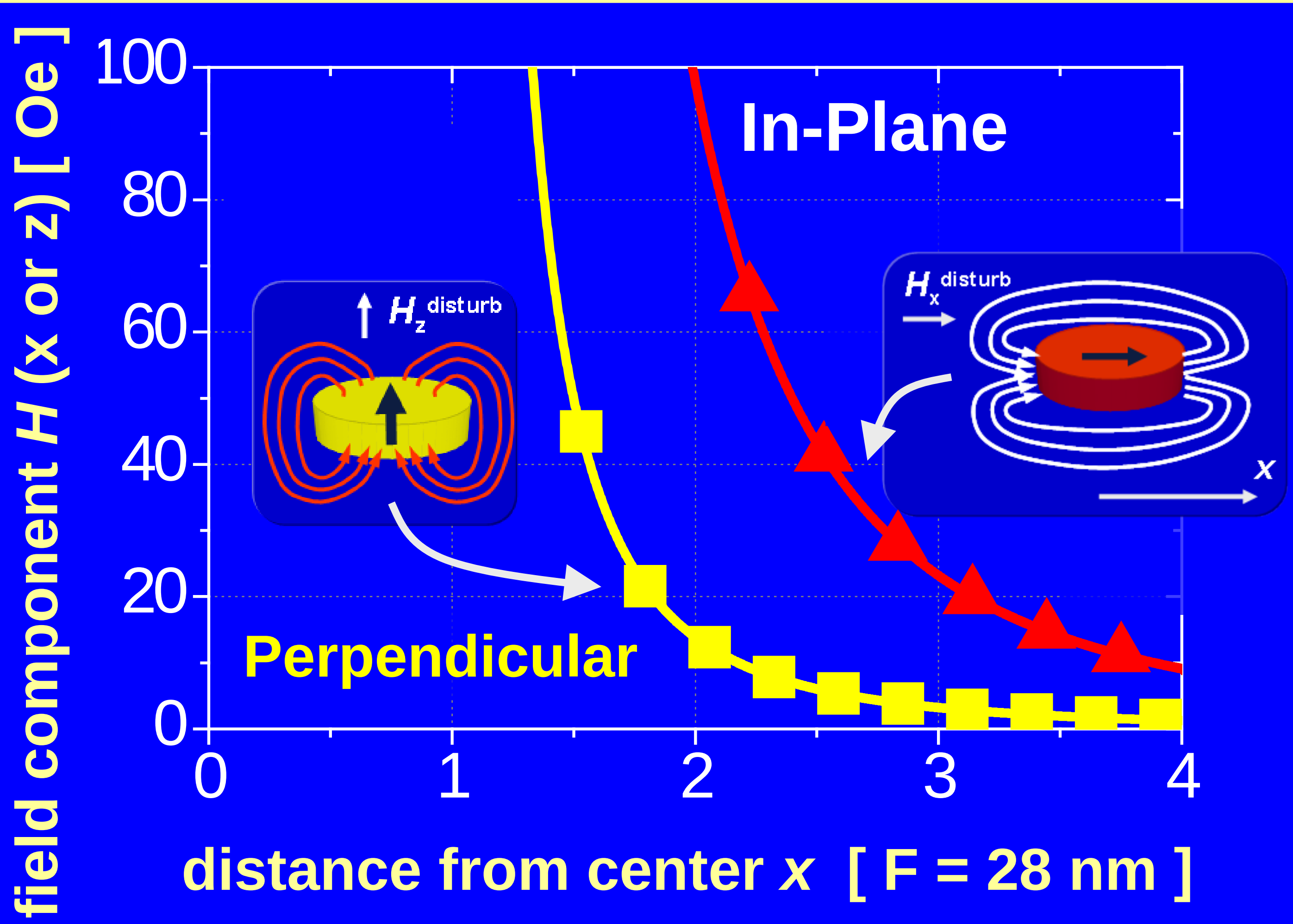
➯ High anisotropy ensures scaling below 20 nm

# Scalability of Switching Current



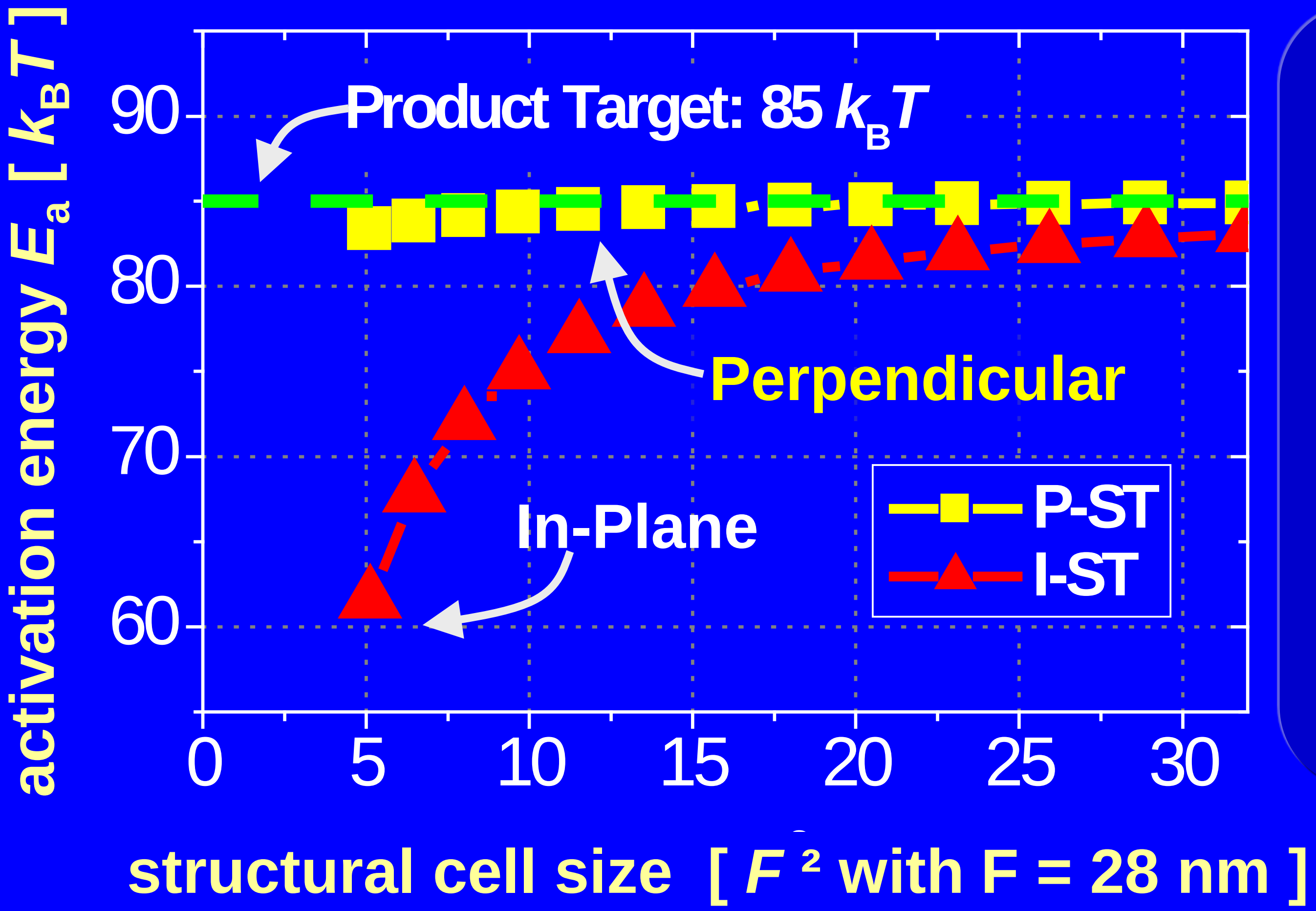
➯ Absence of demagnetization fields reduces required switching current $I_c \sim 30\ \mu A$

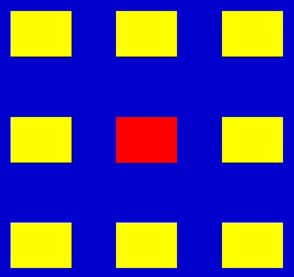
# Cell to Cell Interaction



↳Significantly reduced stray field interaction

# Impact of Interaction on $E_a$



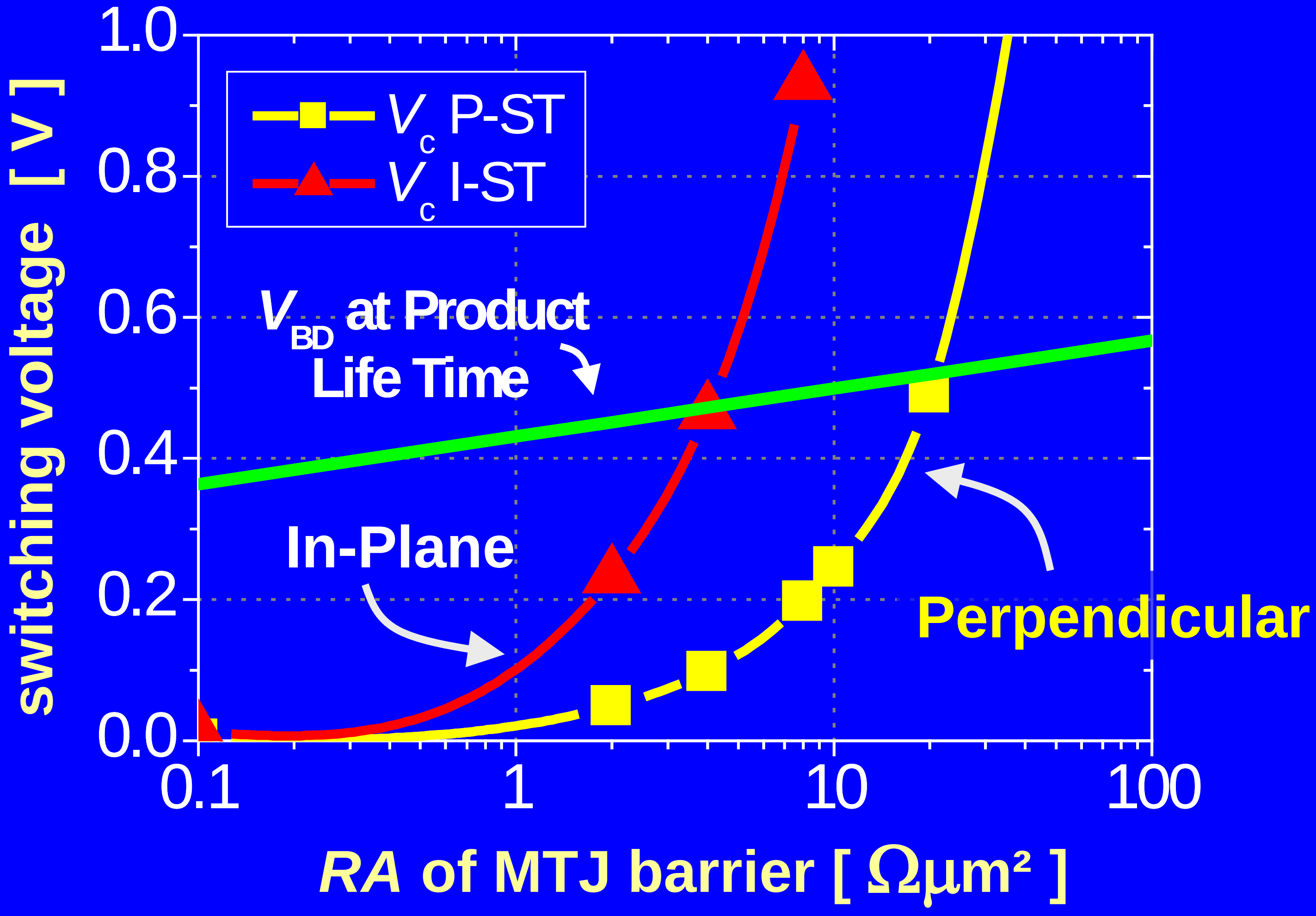


**Correct $E_a$ by**

$$\times\left(1-\frac{H_{disturb}}{H_k}\right)^{\sim 1.5}$$

➥ High data retention at dense spacing

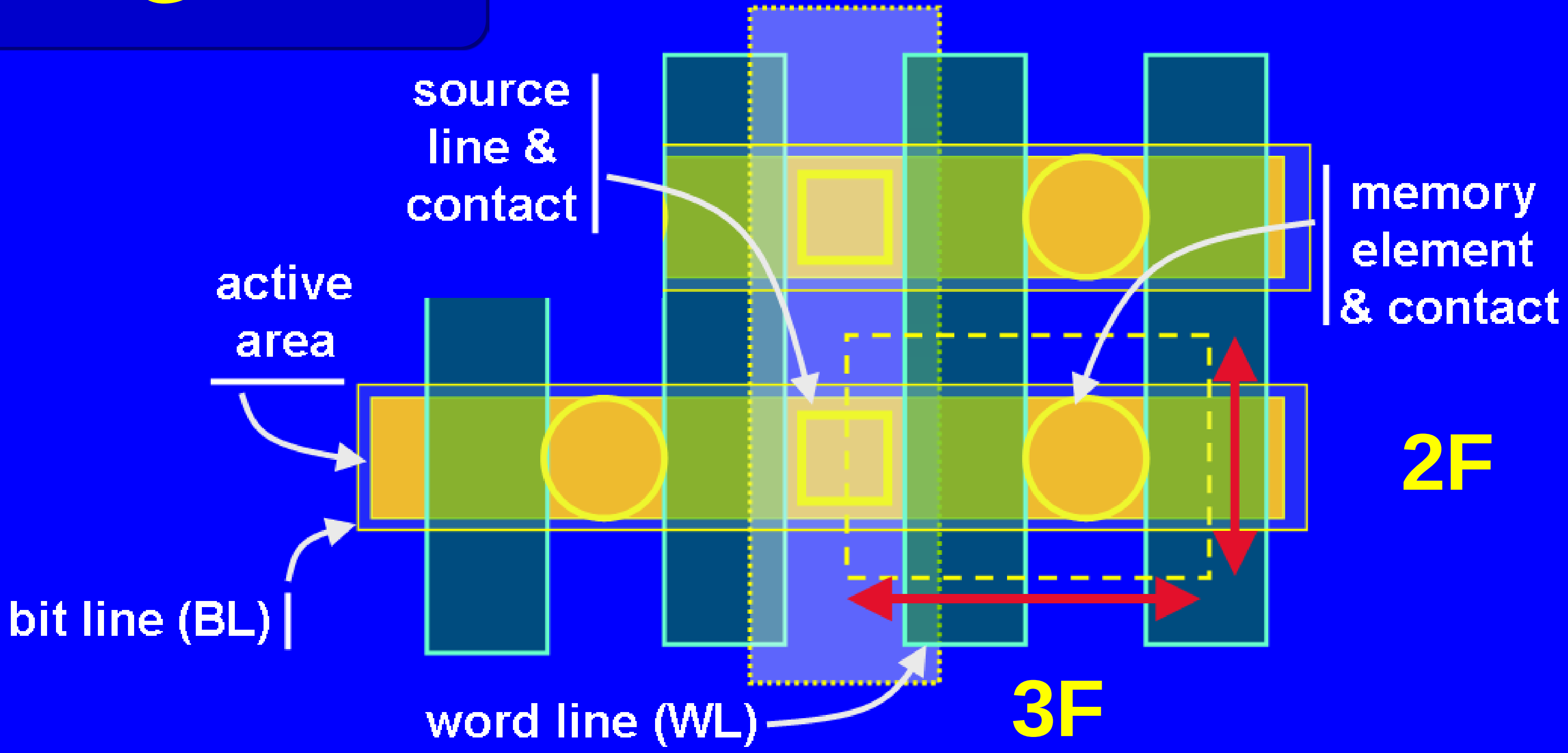
# Reliability Estimates



➯P-ST allows to use high RA for reliable operation

# Cell Layout at 28 nm Node

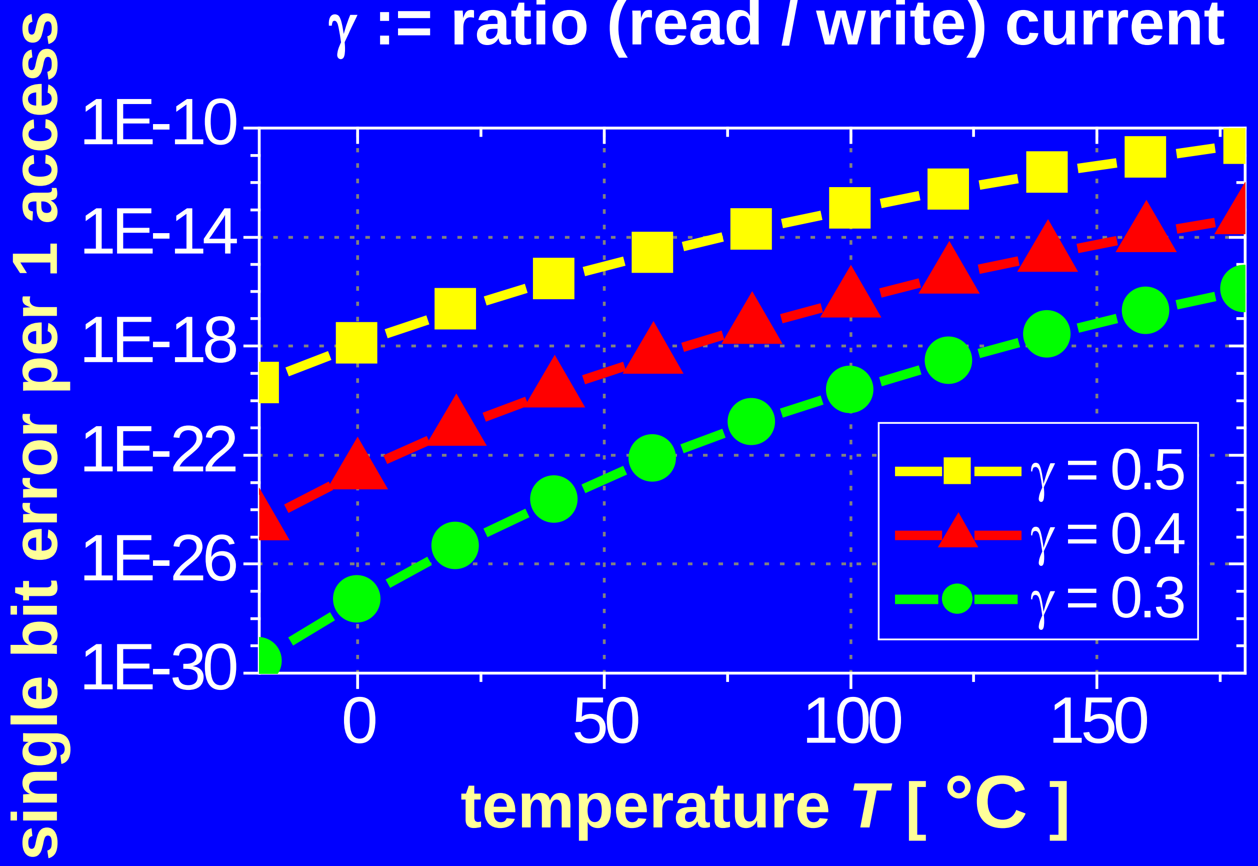
**6 F² @ 28 nm**



↳ 6 F² layout ensures sufficient current drivability

# Read Disturb

γ := ratio (read / write) current

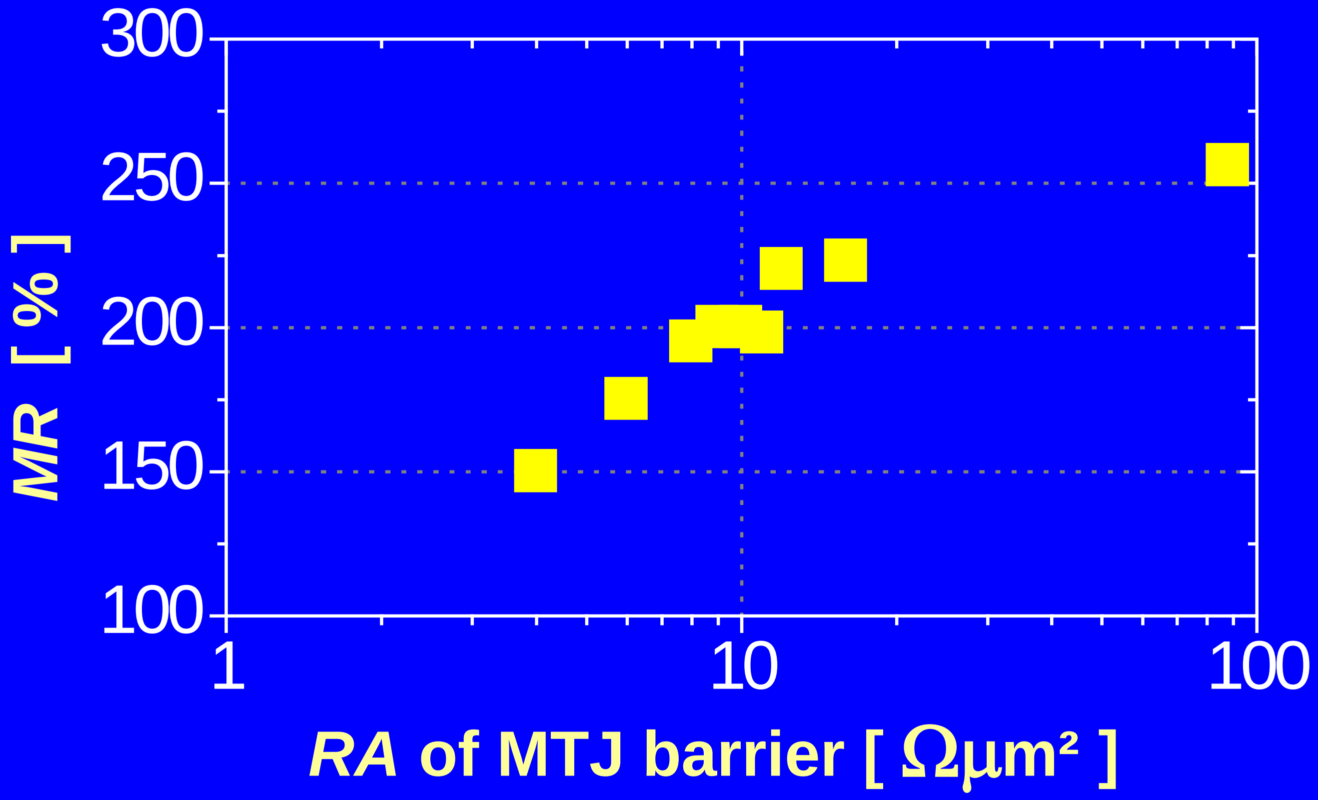


$I_c$ ~ 30 µA

➩ At $I_c$ ~ 30 µA a read current of $I_r$ ~ 10 µA (γ ~ 0.3) is feasible without read disturb

# MTJ Stack Performance

**Measured magneto resistance (MR) for in-plane systems**

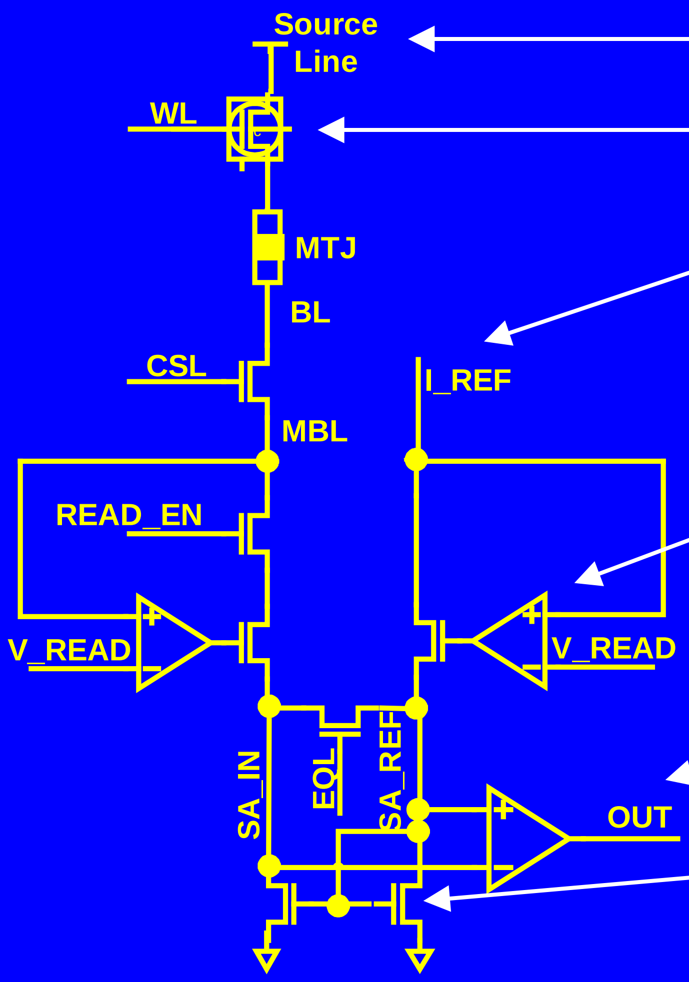


$$MR := (R_1 - R_0) / R_0$$

↳I-ST demonstrated high MR at low RA

↳P-ST will require similar stack performance

# Read Circuit



1.1 V potential

select transistor

reference current

voltage compliance for MTJ: controlling MBL potential by V_READ = 0.95 V

optimized SA

current compliance $I_r$

***Typical:***

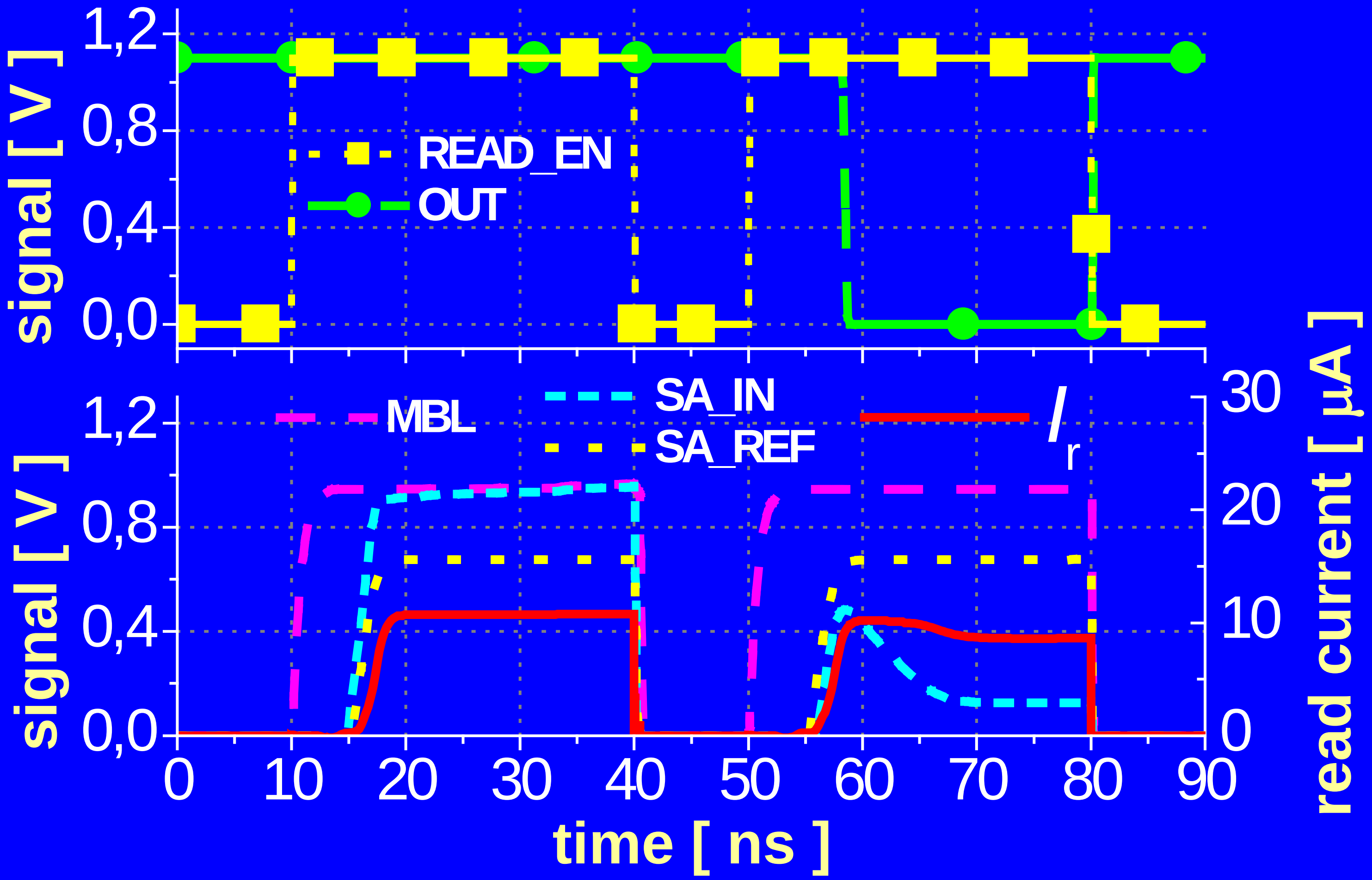
$R_0 = 6\ \mathrm{k}\Omega$

$R_1 = 12\ \mathrm{k}\Omega$

$R_{para} = 14\ \mathrm{k}\Omega$

↳ Current compliance avoids read disturb

# Read Operation Simulation



↳Fast random array read access time ~ 30 ns demonstrated

# Summary

- Perpendicular Spin Torque has been studied targeting the 28 nm node.

- Expected benefits are:
  - long data retention (> 10 yrs @ 85°C)
  - low write current (~ 30 μA)
  - small cell sizes (~ 6 $F^2$)
  - high write endurance and no read disturb

- Random access speeds are 30 ns for read and 10 ns for write.