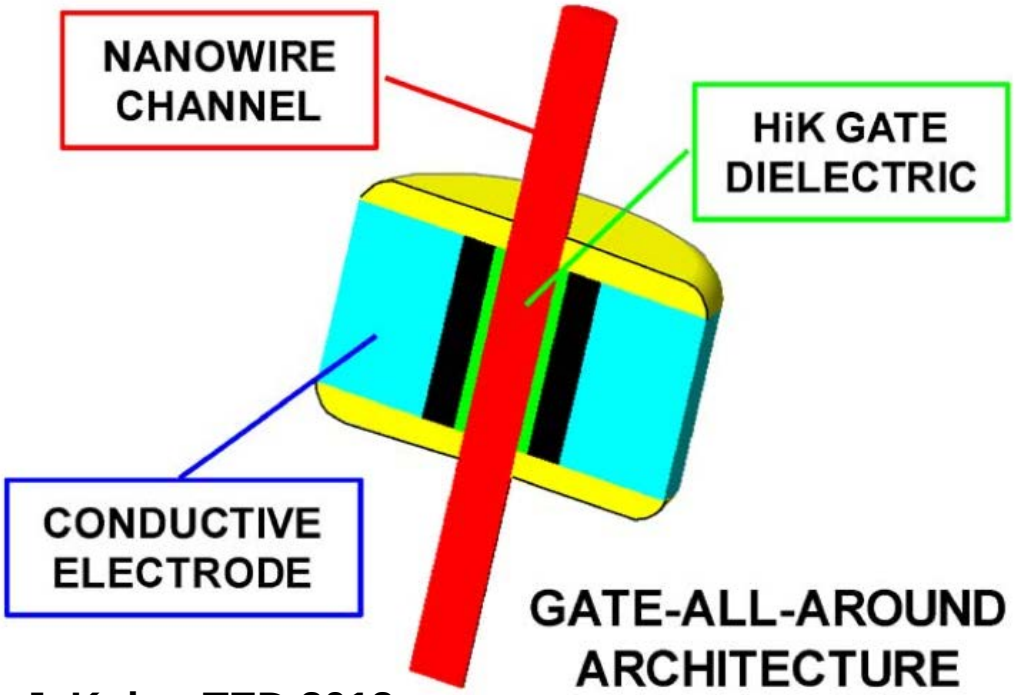
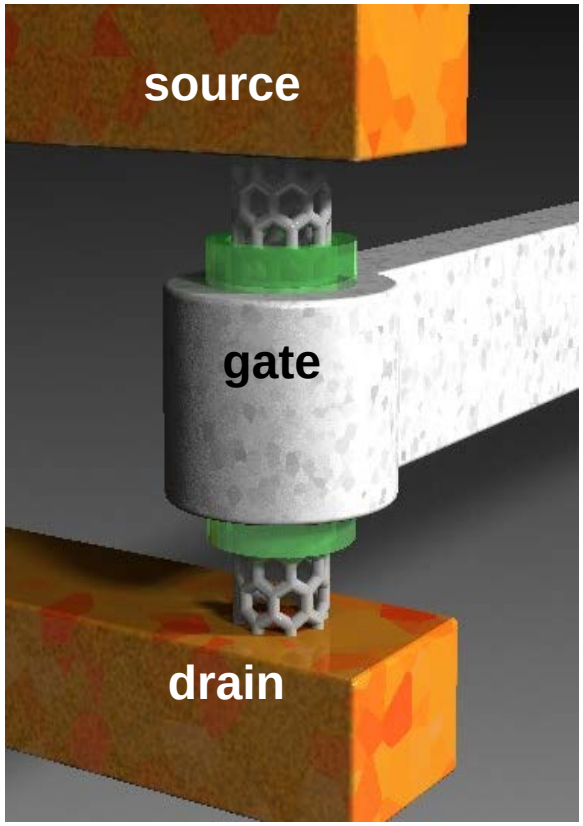
New materials on horizon for advanced logic technology in mobile era



Kelin J. Kuhn, TED 2012

Basic components of the ultimate CMOS device.

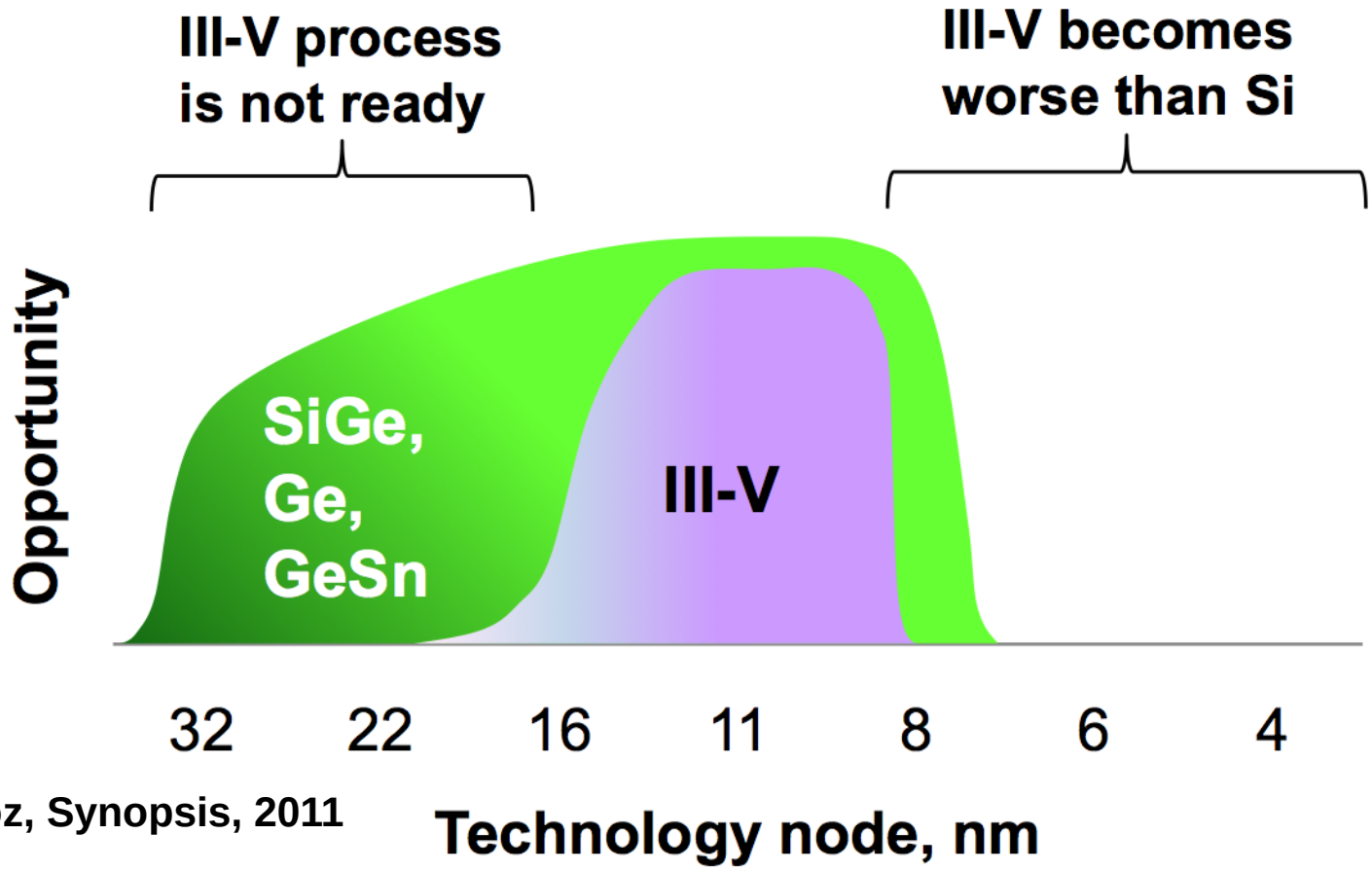


Franz Kreupl, IFX 2003

Outline

- Introduction
- Comparing carbon nanotubes with our wish list for the "switch of the future"
- Bridging the gap:
  Show a strategy how to bring nanotubes into the semiconductor eco-system
- Conclusions

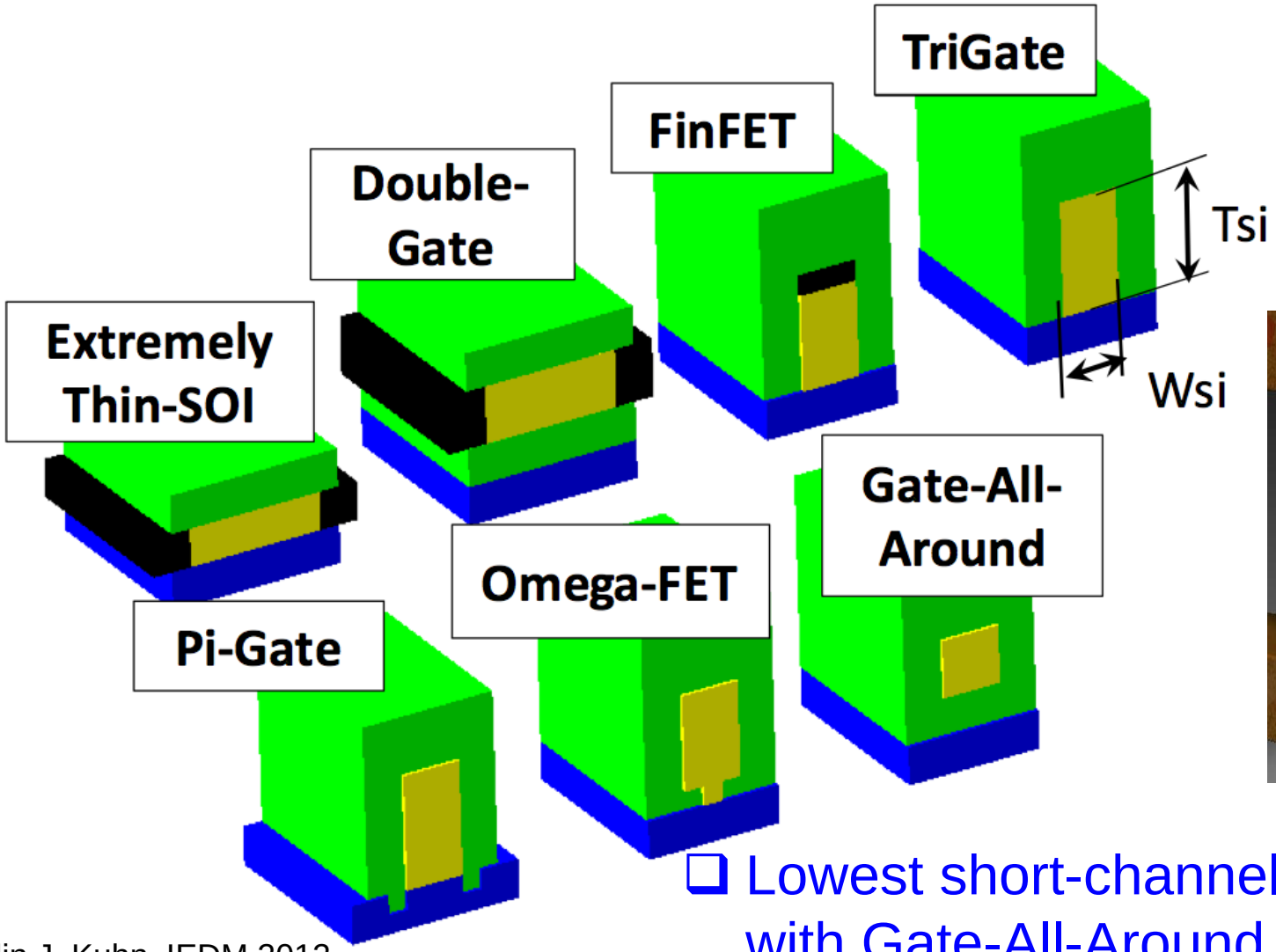
Limited time window for alternatives

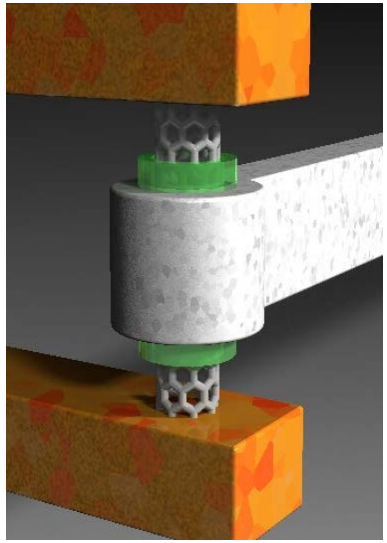


V. Moroz, Synopsis, 2011

- Si-based CMOS is still the mainstream for downsizing to sub-10 nm.

Electrostatics favors gate-all-around



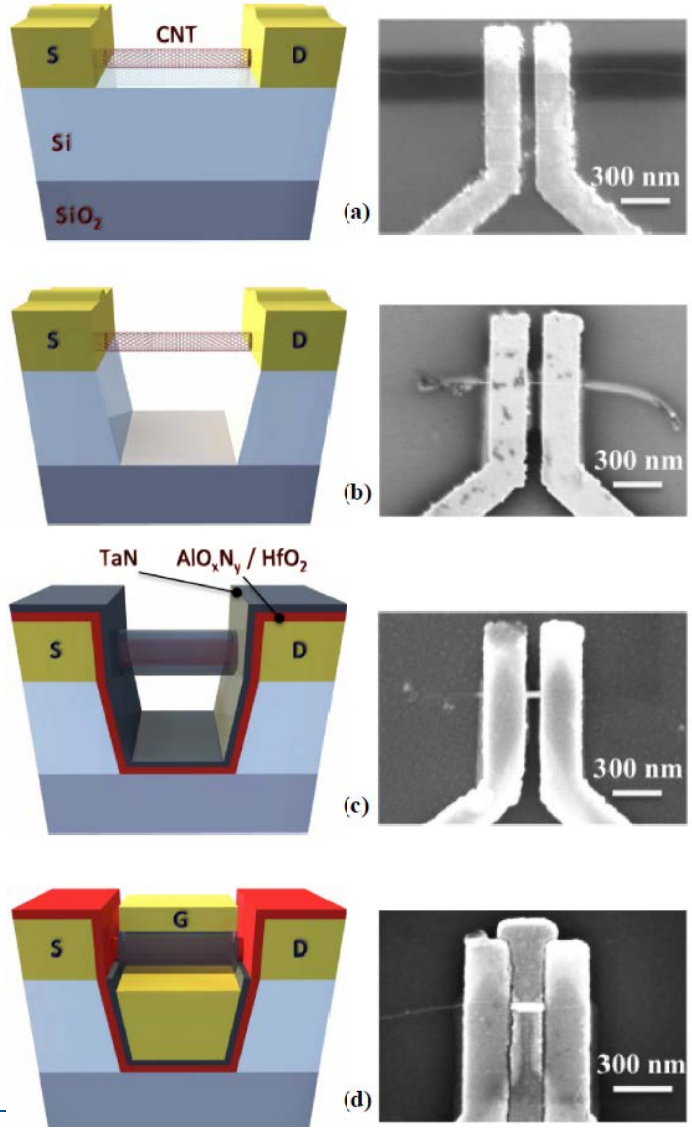


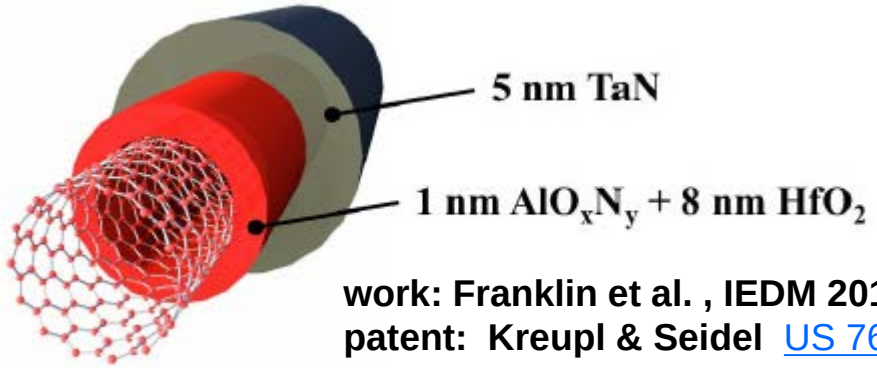
Franz Kreupl, IFX 2003

- Lowest short-channel effects with Gate-All-Around

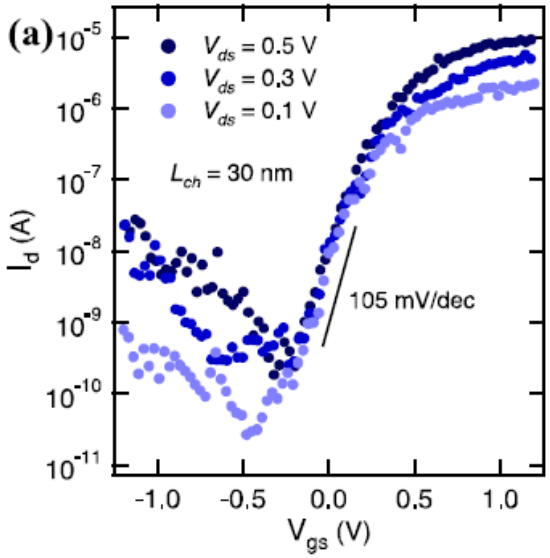
Kelin J. Kuhn, IEDM 2012

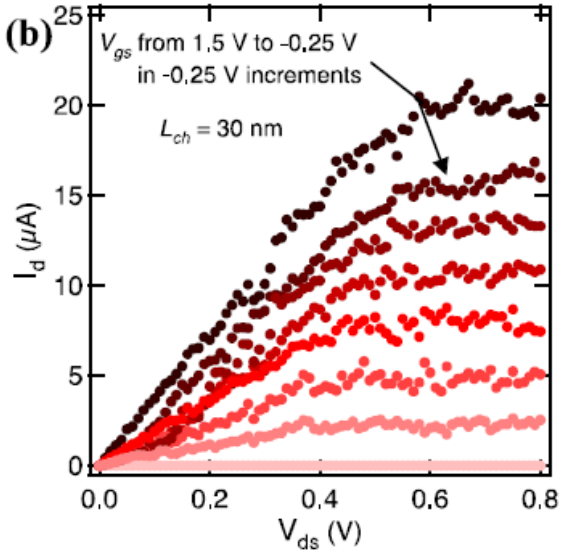
Carbon nanotubes do gate-all-around





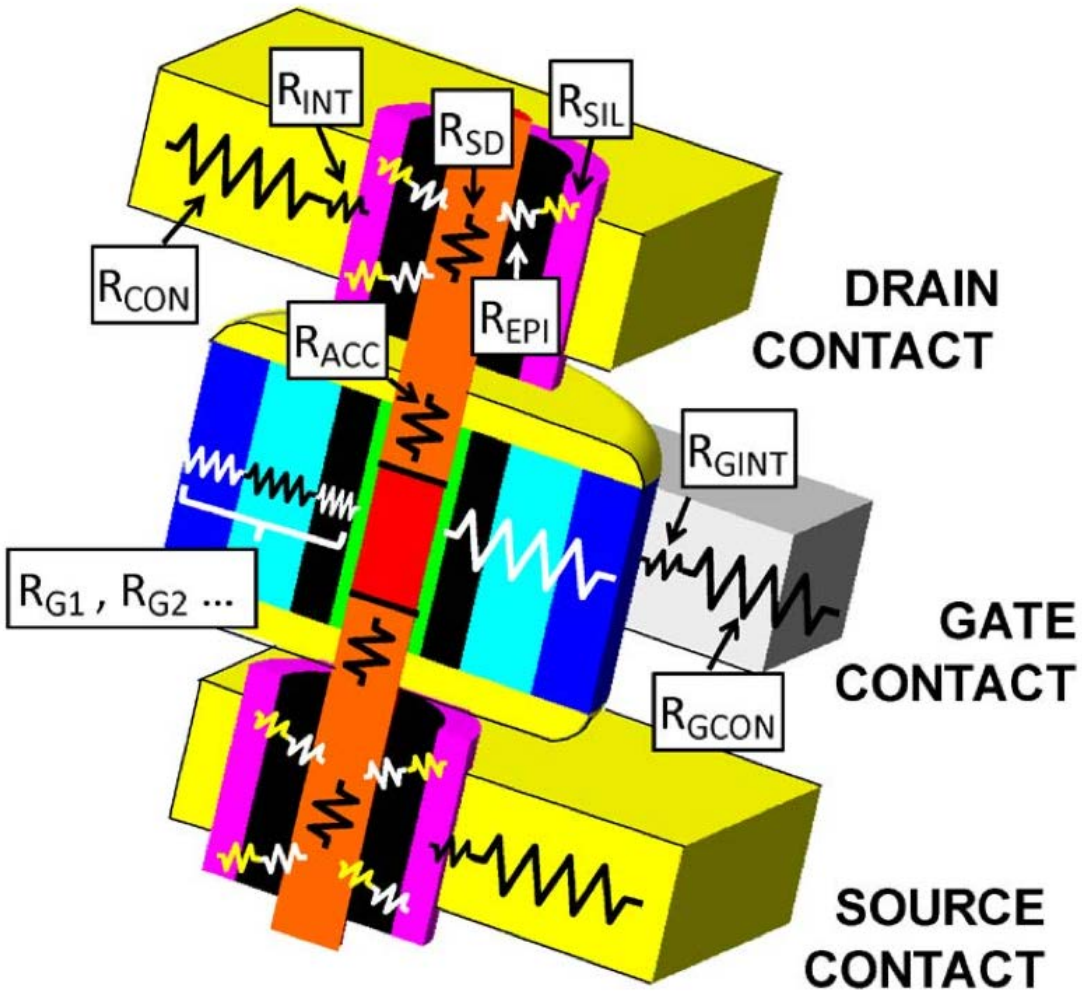
work: Franklin et al. , IEDM 2012
patent: Kreupl & Seidel US 7646045



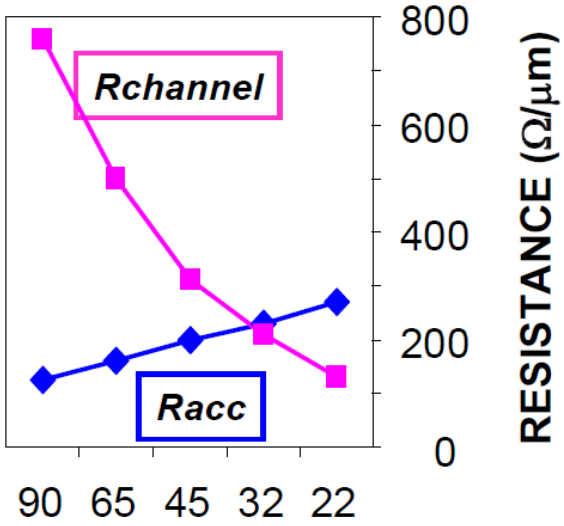


- Very high on-current
- No/low DIBL

Contact resistance: major headache



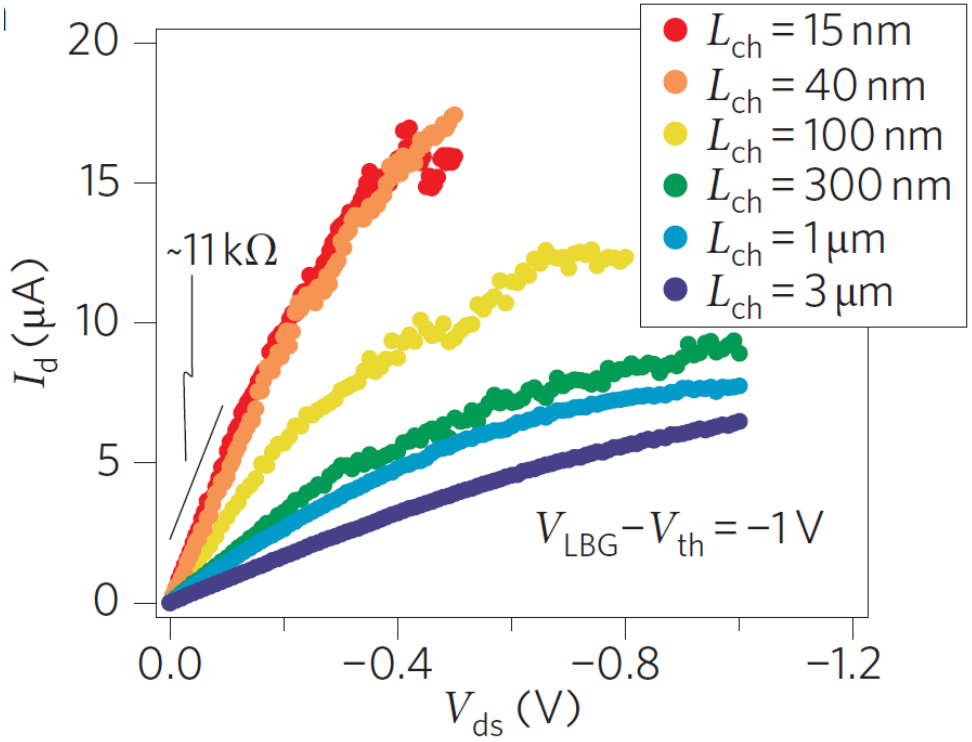
Kelin J. Kuhn, TED 2012



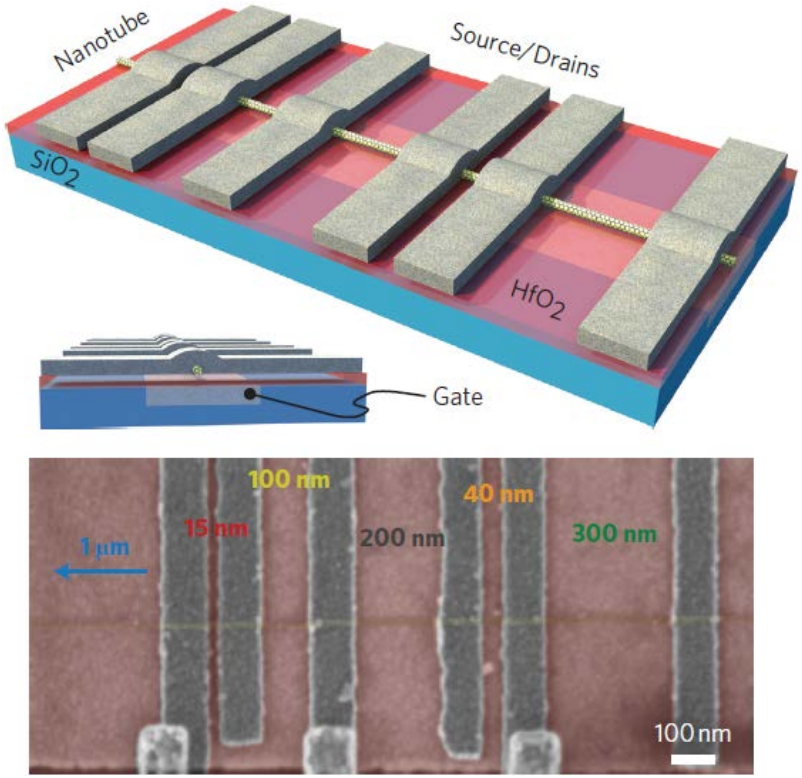
A.M. Noori, AMAT, TED 2008

- At 10 nm half-pitch **one contact** will be > 30 kOhm
- would like purely **metallic contacts**

Carbon nanotubes do have metallic S/D

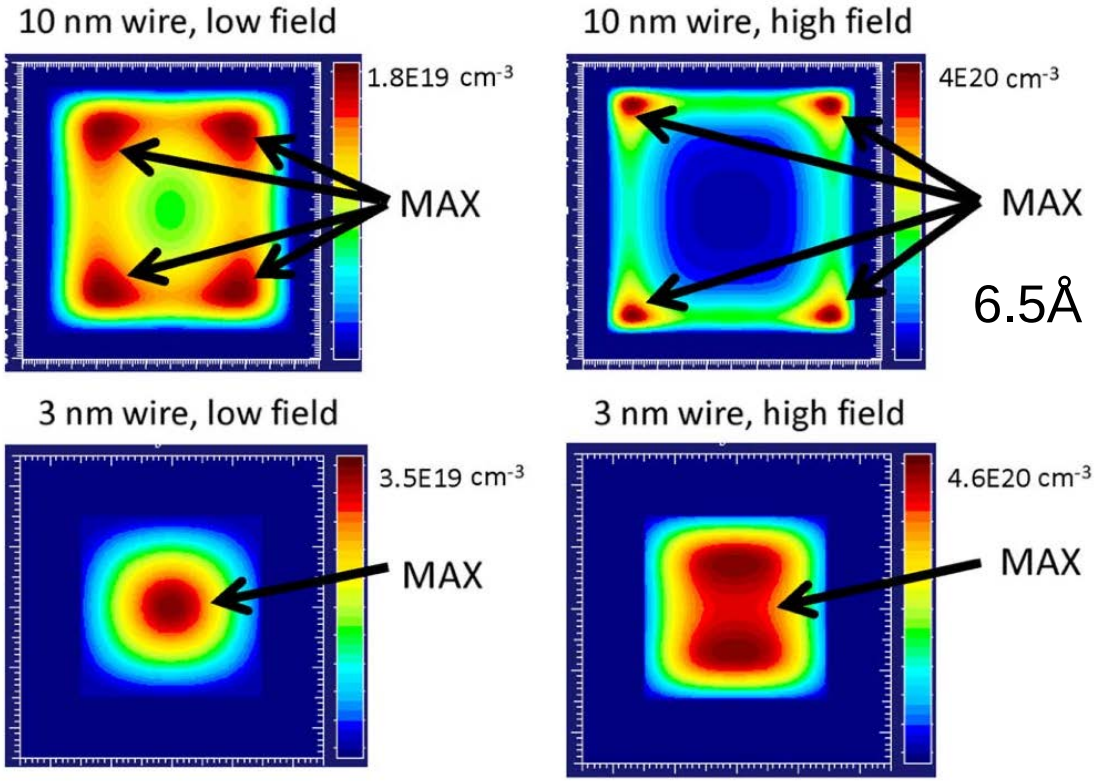


Franklin et al, Nature Nano 2010

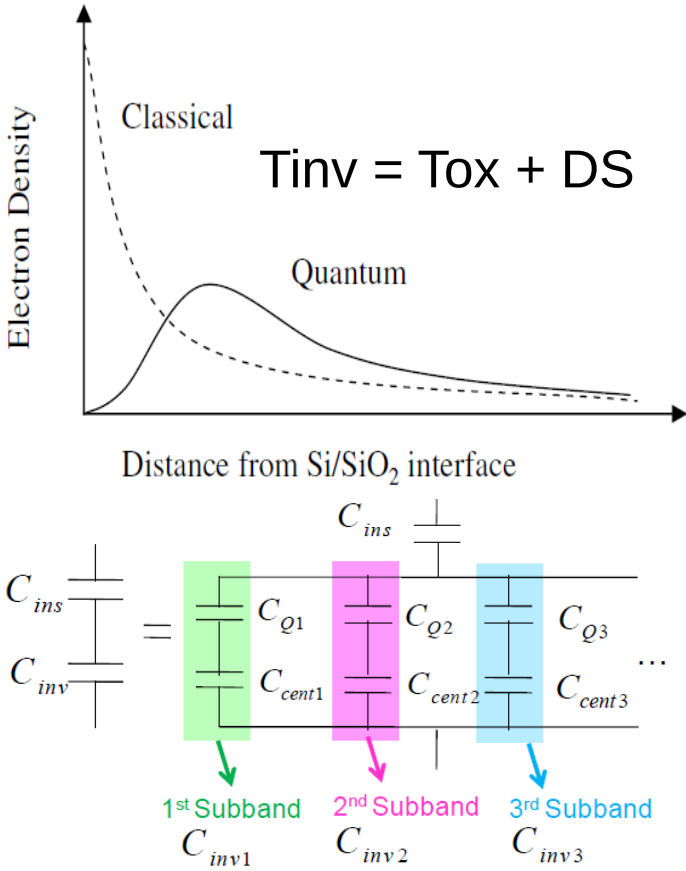


- One contact to 1 nm wide channel will be ~ 5.5 kOhm
- Short channel (15-40 nm) operates in the ballistic limit
- Type of metal defines p- or n-type channel

Dark space in silicon / high-μ channels



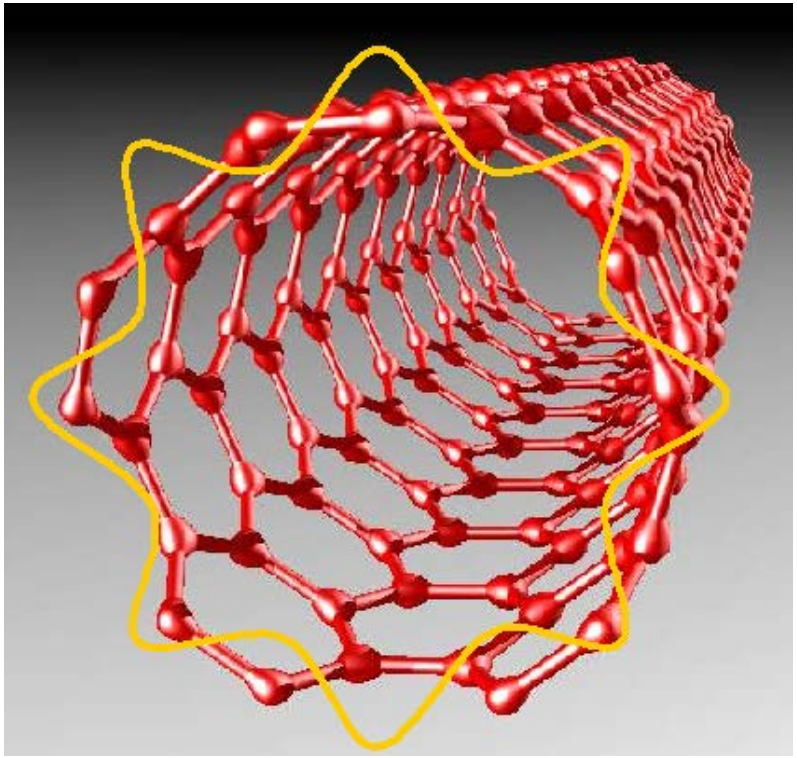
in Silicon Kelin J. Kuhn, TED 2012



- Dark space gets worse due to reduced DOS – C_{inv} α 1/DOS
- Severe limiter for channel control ➔ SS / DIBL deterioration

Skotnicki & Boeuf, **VLSI 2010**

Carbon Nanotubes have no dark space

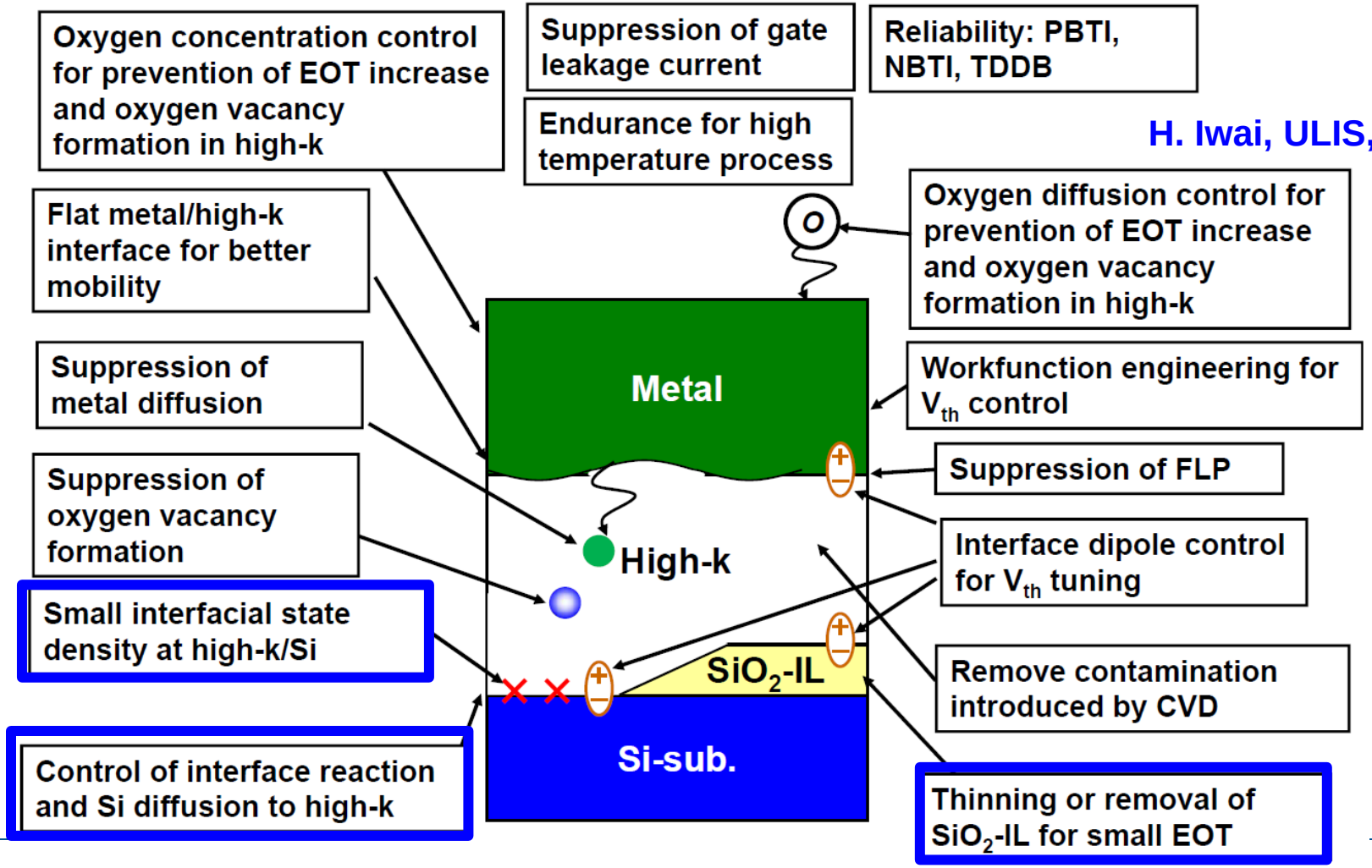


- Current is confined to a single atomic layer
- Intimate channel control & low DOS
- Operation in the quantum capacitance limit (QCL) possible
- In QCL, the potential in channel is determined by the gate potential
- short channel effects are suppressed
- Nanotube have no dopants

c.f. Knoch et al. EDL, 2008

Channels need high-k compatibility

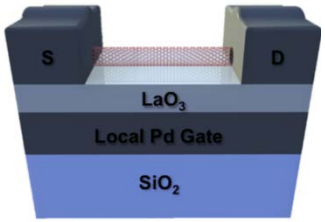
Issues in high-k/metal gate stack

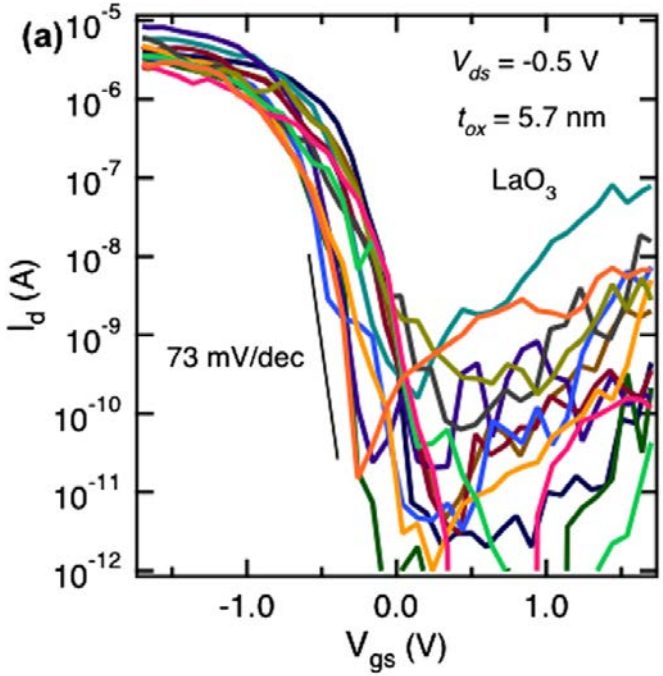


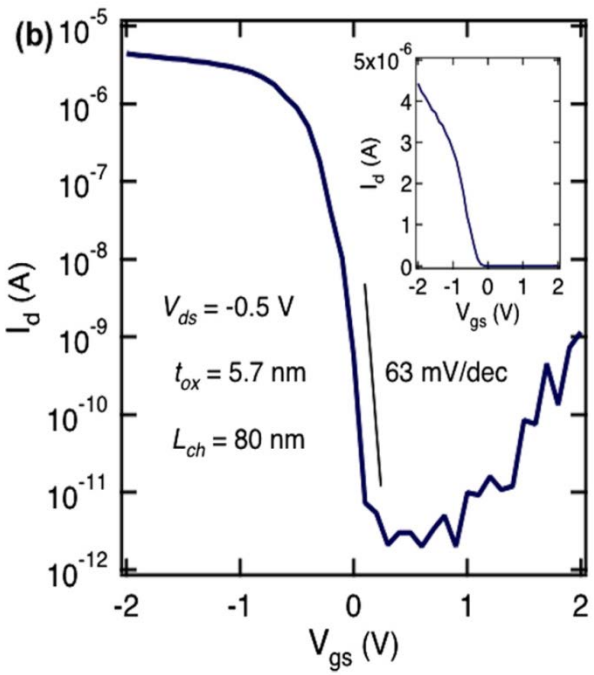
Carbon Nanotubes are high-k compatible

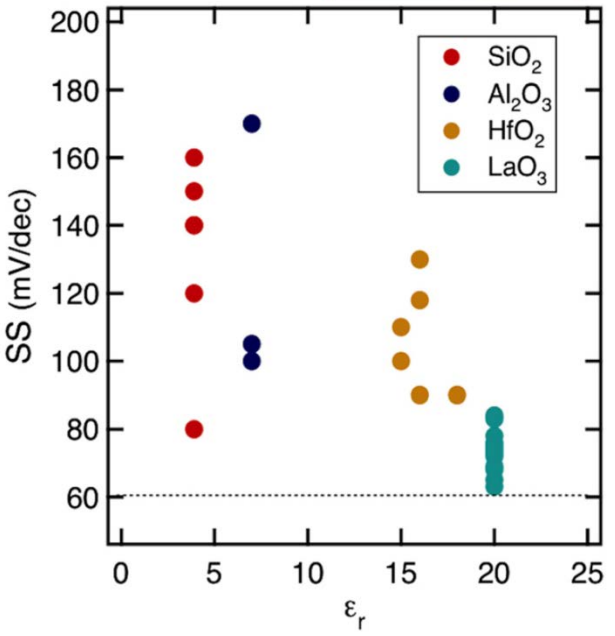
- No dangling bonds
- Low chemical reactivity

} High-k materials are easily employed









A. Franklin, APL, 2013

- lanthanum oxide looks very promising

Si performance vs L_{gate} and voltage scaling

	Intel (IEDM2007, 2009)		Intel (VLSI2012)	Toshiba (VLSI2012)	IBM (VLSI2012)	Samsung (IEDM2012)	IBM (IEDM2009)	STMicro. (VLSI2008)	Tokyo Tech (ESSDERC2010)
Structure	Bulk Planar		Tri-Gate 22nm	Tri-Gate NW	ETSOI	Bulk Planar	GAA NW	GAA NW	Ω-gate NW
	45nm	32nm							
L_g (nm)	35	30	30	14	22	20	35/25 (nFET/pFET)	22/30 (nFET/pFET)	65
Gate Dielectrics	Hf-based		Hf-based	SiO_2	HfO_2	HfO_2 ?	Hf-based	$HfZrO_2$	SiO_2
EOT (nm)	1	0.95	0.9	3	~1	-	1.5	-	3
V_{th} (V)	~0.4	~0.3	~0.2	-0.15 (nFET)	0.3~0.4	~0.3	0.3~0.4	~0.5	-0.2 (nFET)
V_{DD} (V)	1	1	0.8	1	1	0.9	1	1.1	1
I_{ON} (mA/um) nFET/pFET	1.36/1.07	1.53/1.23	1.26/1.1	0.83 (nFET)	1.65/1.25	1.2/1.05	0.83/0.95	2.05/1.5	1.32 (nFET)
DIBL (mV/V) nFET/pFET	~150	~200	46/50	<50	75/130	104/115	65/105	56/9	62
SS (mV/dec)	-	~100	~70	<80	<90	87	85	<80	70

Iwai & Salvo, ISCDG 2012

- No data at low Vds (0.5V) and short Lgate

III-V/Ge benchmark – only long Lgate

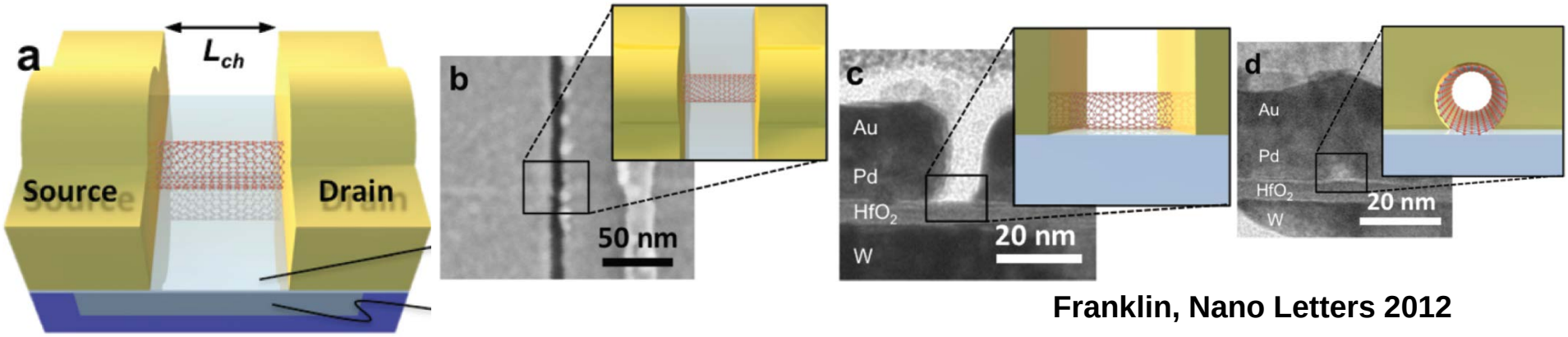
	Planar (metal S/D, Strain, Buffer…)			FinFET		Tri-gate		Gate-all-around MOSFET		Nanowire	
material	InGaAs	Ge	InGaSn	InGaAs	Ge	InGaAs	Ge	InGaAs	Ge	InGaAs (multishell)	Ge
Dieletric /EOT	Al_2O_3/ 3.5 nm	7.6 A° HfO_2+ Al_2O_3+GeO_2	5nm ALD Al_2O_3	5nm ALD Al_2O_3	SiON	1.2 nm	5.5 nm (Al_2O_3+ GeO_2)	10nm-ALD Al_2O_3	HfO_2: 11nm	HfAlO 14.8 nm	3.0 nm (ALD Al_2O_3)
Mobility	-	~600 (cm^2/Vs)	N_s: 5e12 e: 200 h: 400 (cm^2/Vs)	~700 (μS/μm)	-	-	-	701 (μS/μm)	-	~500 (μS/μm)	~850 (cm^2/Vs)
L_{ch} (nm)	55	W/L= 30/5 μm	50 μm	100	4.5 μm	60	183	50	200	200	65
DIBL (mV/V)	84	-	-	180	-	~50	-	210	-	-	-
SS (mV/dec)	105	-	150K 61pMOS 33nMOS 120K	145	750	90	130	150	160	-	-
I_{ON} (μA/μm)	278 (V_D=0.5V)	3 (V_D=-0.2V)	4 (n,p) (V_D=0.5V)	-	10 (V_D=0.5V)	400 (V_D=0.5V)	235 (V_D=-1V)	180 (V_D=0.5V)	604 (V_D=-0.5V)	100 (V_D=0.5V)	731 (V_D=-1V)
Research Group	Tokyo Uni VLSI 2012	Tokyo Uni VLSI 2012	Stanford Uni VLSI 2012	Purdue Uni IEDM 2009	Stanford Uni ELD 2007	Intel IEDM 2011	NNDL Taiwan IEDM 2011	Purdue Uni IEDM 2011	ASTAR Singapore IEDM 2009	Hokkaido Uni, IEDM 2011	AIST Tsukuba VLSI 2012

Iwai & Salvo, ISCDG 2012

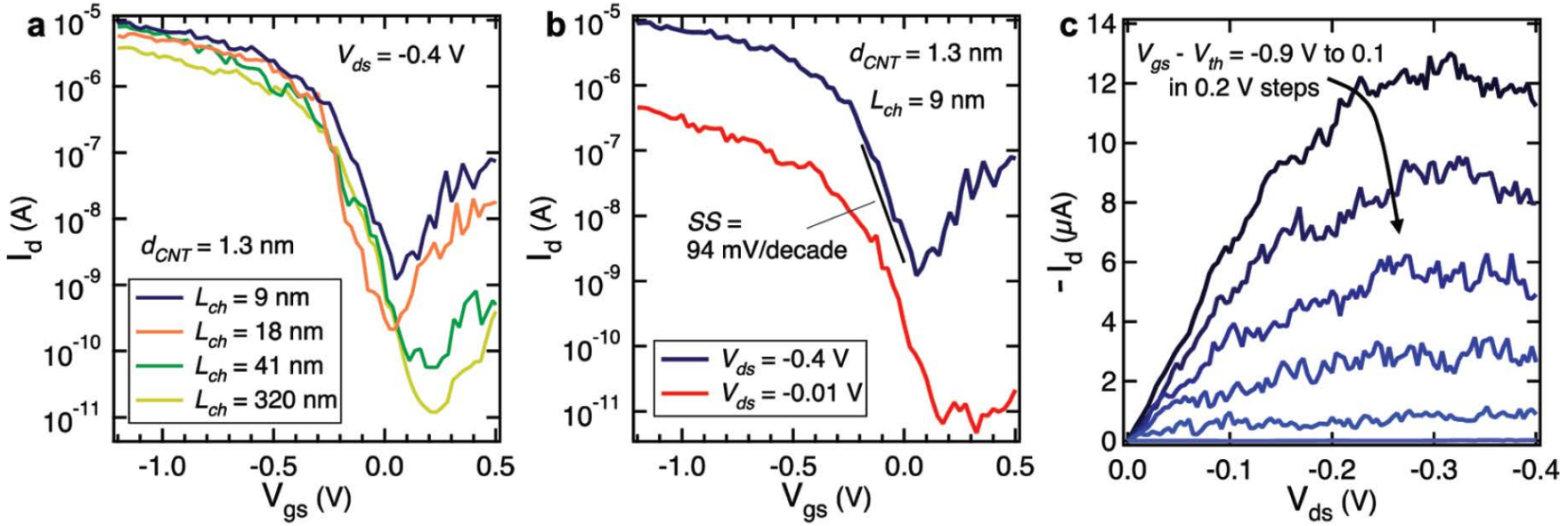
31

- No data at low Vds (0.5V) and short Lgate

Sub-10 nm carbon nanotube transistor

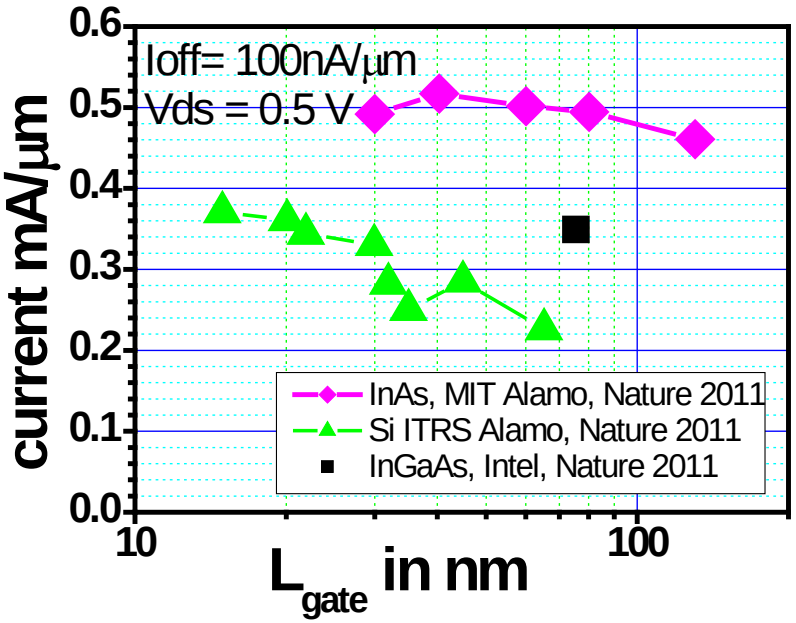


Franklin, Nano Letters 2012

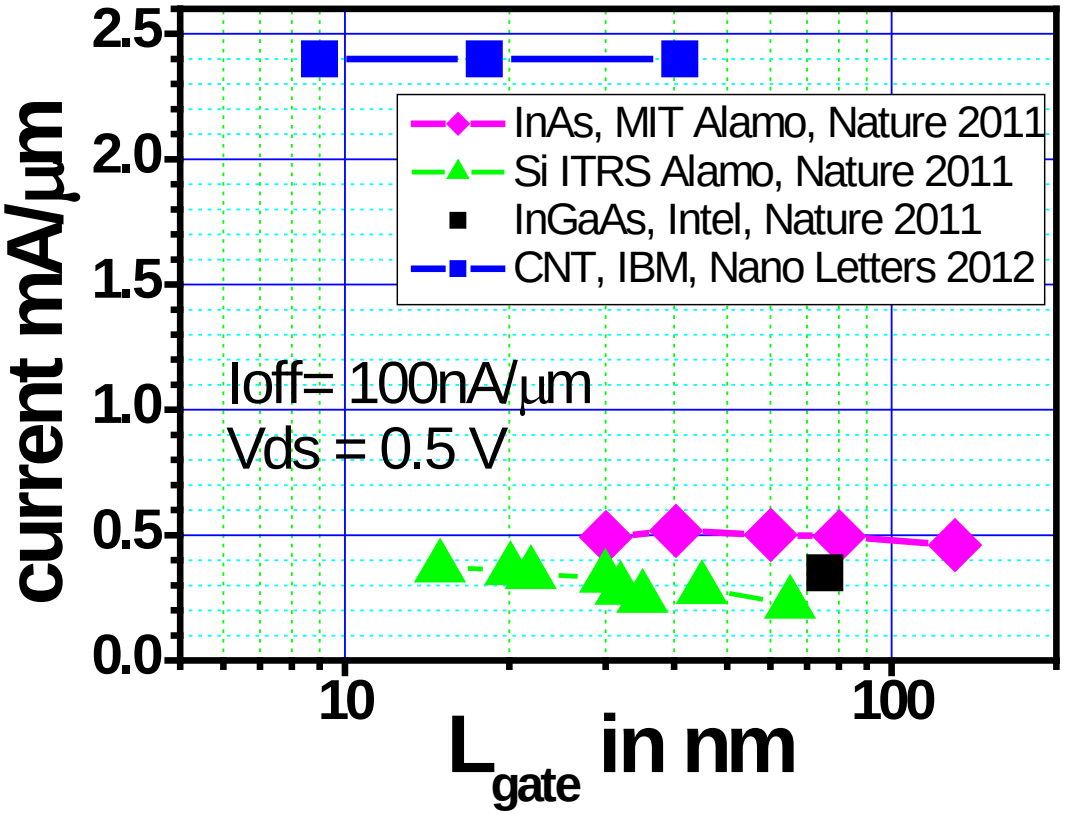


Operation at low Vds (0.4V) and short Lgate of 9 nm

Carbon nanotubes outperform alternatives



Jesus Alamo, Nature 2011

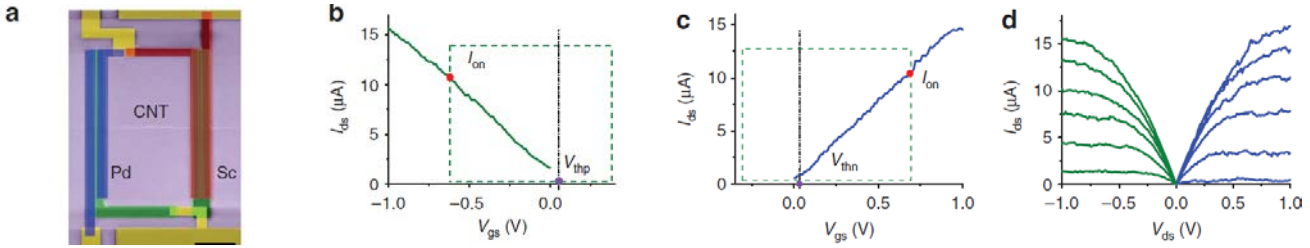


CNT Ioff: 1000nA/µm for 9nm !
100nA/µm for >= 18nm

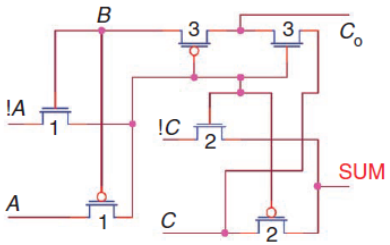
"Carbon nanotubes finally deliver"

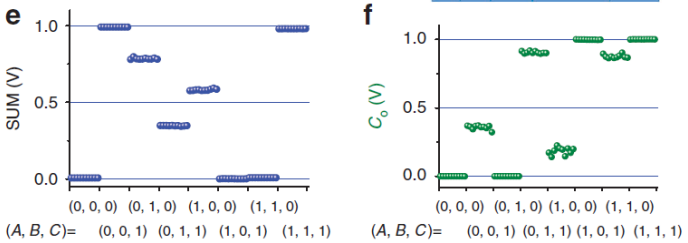
Advantage for CNTs in circuit designs

- CNT-based ICs can be designed as pass-transistor logic (PTL),



- Drawback of conventional Si-based PTL circuits—threshold voltage drop—is avoided in CNT PTL circuits
- Threshold voltage can be adjusted close to zero for p- and n-CNT FET (operation at Vdd= 1 and 0.4 V demoed)
- number of FETs & power greatly reduced / enhanced speed
- **Full adder**: instead of 28 FETs (in Si) only 6 CNT FETs

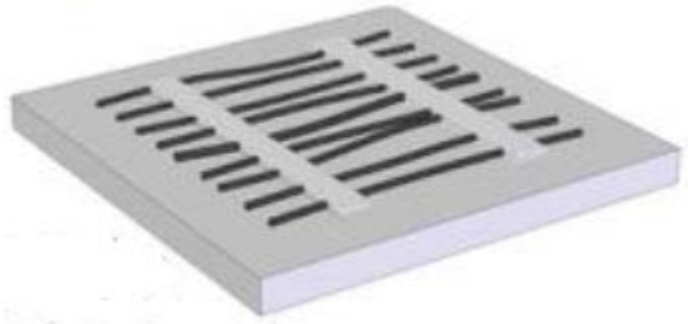




Ding, L. et al., Nature Com. 2012

Great News – how to proceed?

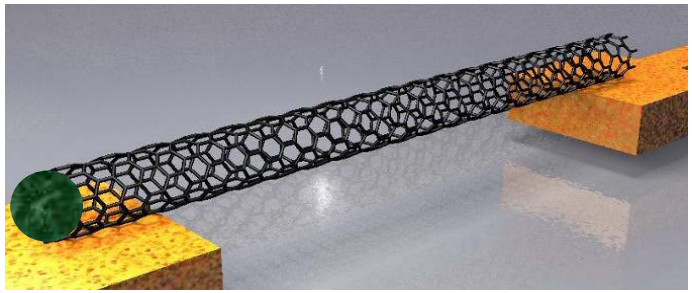
- Please give instructions
  - ➔ how to place billions of nanotubes with
    - one type of chirality
    - equal length
    - on a substrate
    - well aligned at some nanometer pitch
    - with a throughput of 120 wafers per hour



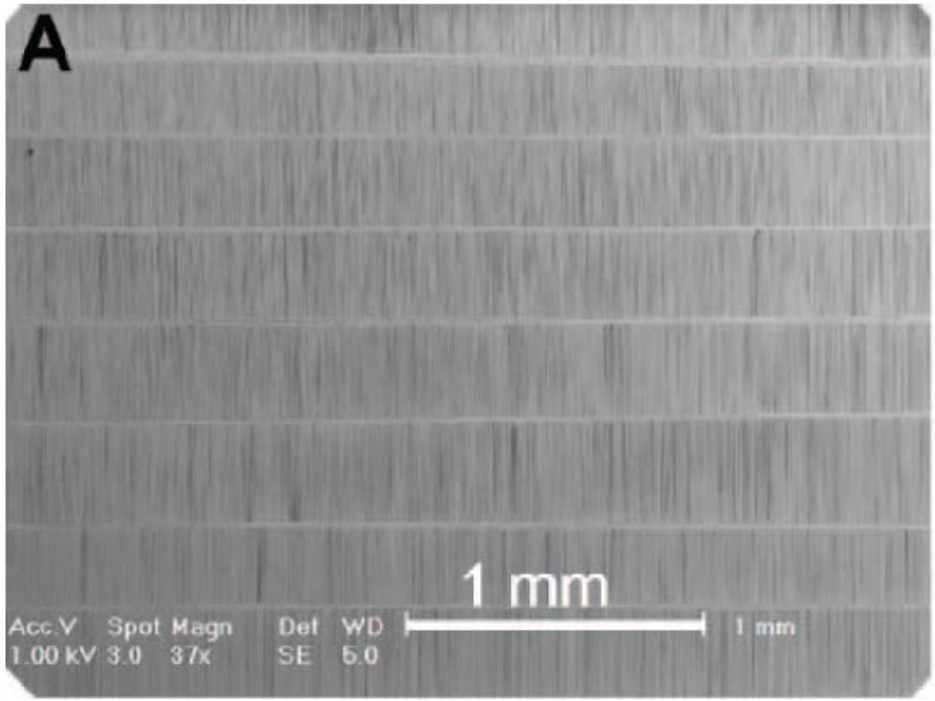
- **Solution**: Just issue a purchase order for the new Applied Materials ***Nano-Wonder™*** machine

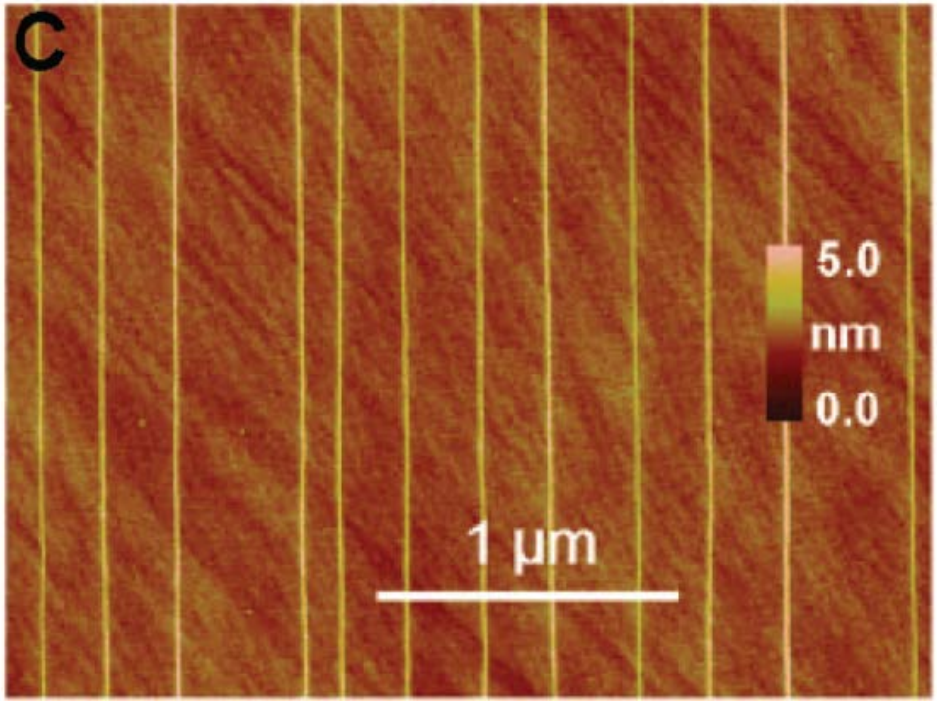
No - unfortunately – I am kidding

Placement strategies



- Grow in place or transfer
  - 95 % semiconducting CNTs possible (Lei Ding et al, NL 2009)

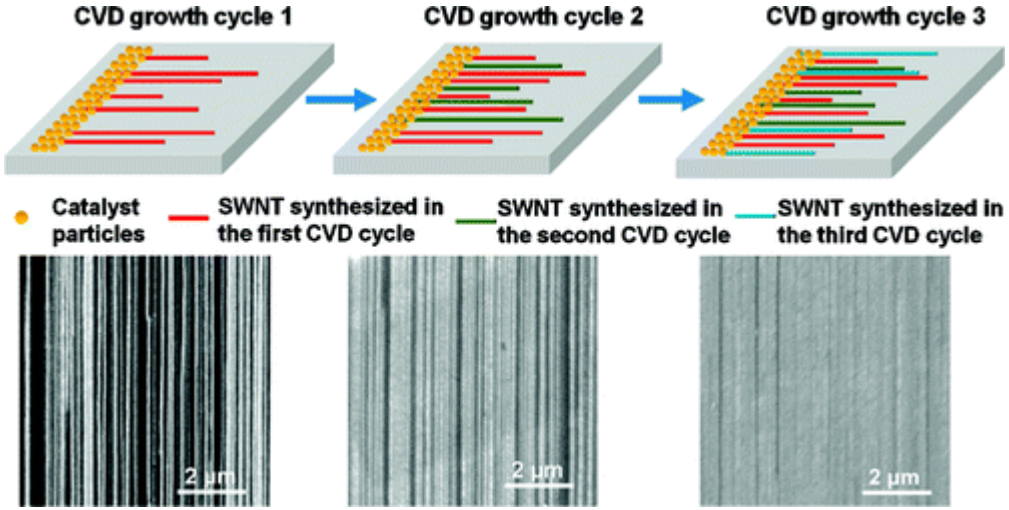




- aligned growth is possible – pitch not (yet) suitable

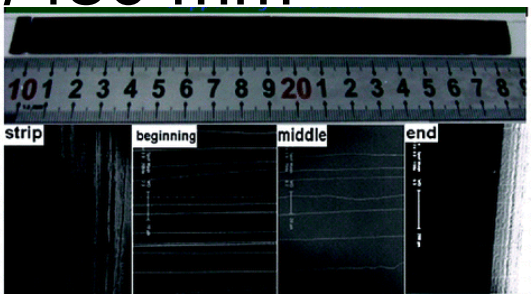
Placement strategies

- Grow in place or transfer
  - density can be increased by multiple growth



W Zhou et al., J. ACS Nano, 2011

- Would work if growth length is > 300 /450 mm
  - Longest grown nanotube is 18.5 cm
  - Metallic could be eliminated (new methods)
  - Poor control over chirality



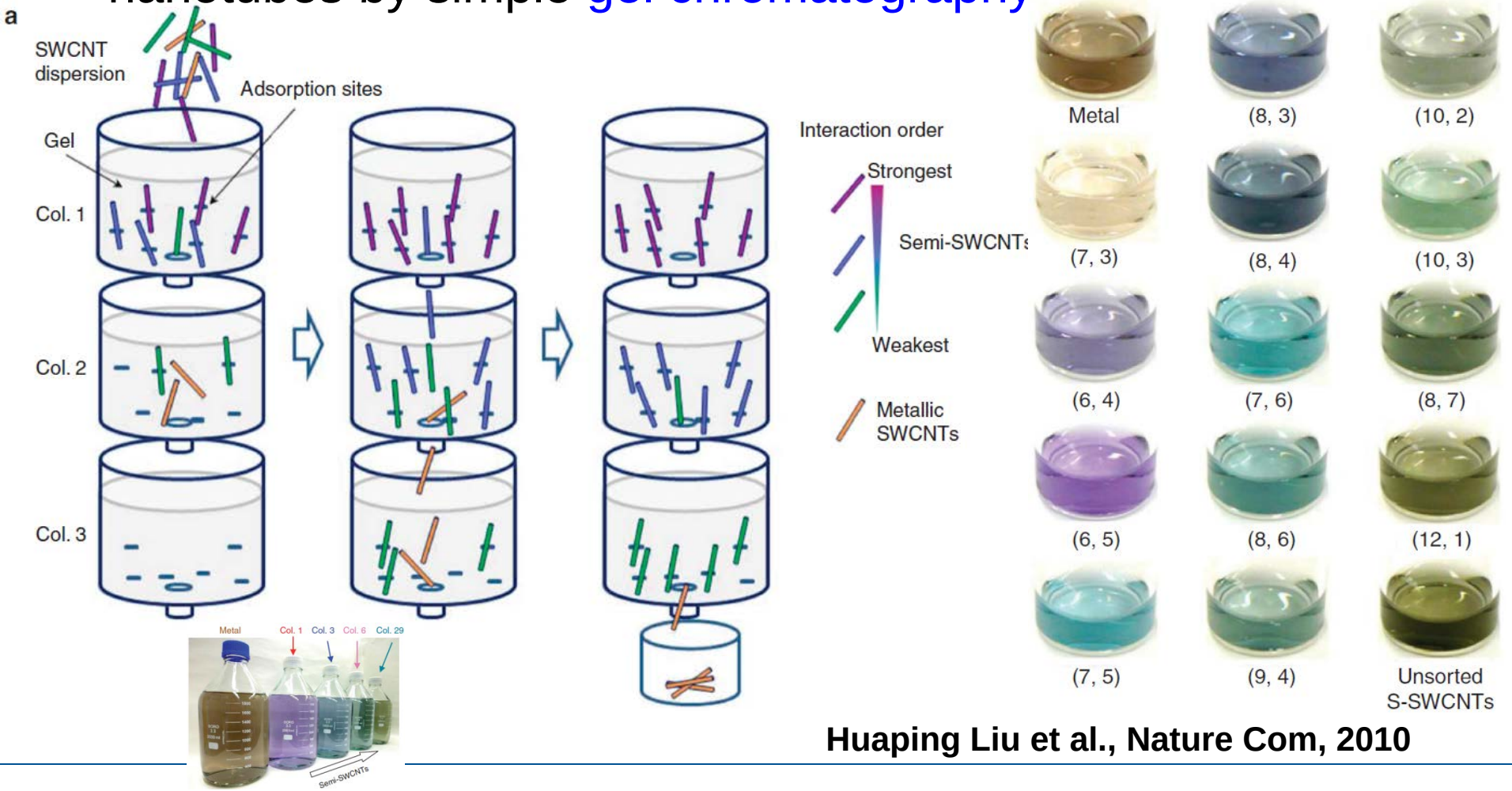
Xueshen Wang et al, Nano Let. 2009

Placement strategies

- Use **self-assembly** to place nanotube
- Key ingredient: only semiconducting nanotubes
  - Bulk produced single-walled nanotubes (HiPCo etc)
  - Large-scale single-chirality separation of single-wall carbon nanotubes by simple gel chromatography or density gradient or DNA methods
  - cloning of specific chirality - may be omitted
- Develop a site specific selective binding to deposit nanotubes at specific location
- Start integration work / fabrication of the devices
- Evaluate (millions of) devices
- Feedback and improve process – start again

Placement strategies

- Large-scale single-chirality separation of single-wall carbon nanotubes by simple gel chromatography

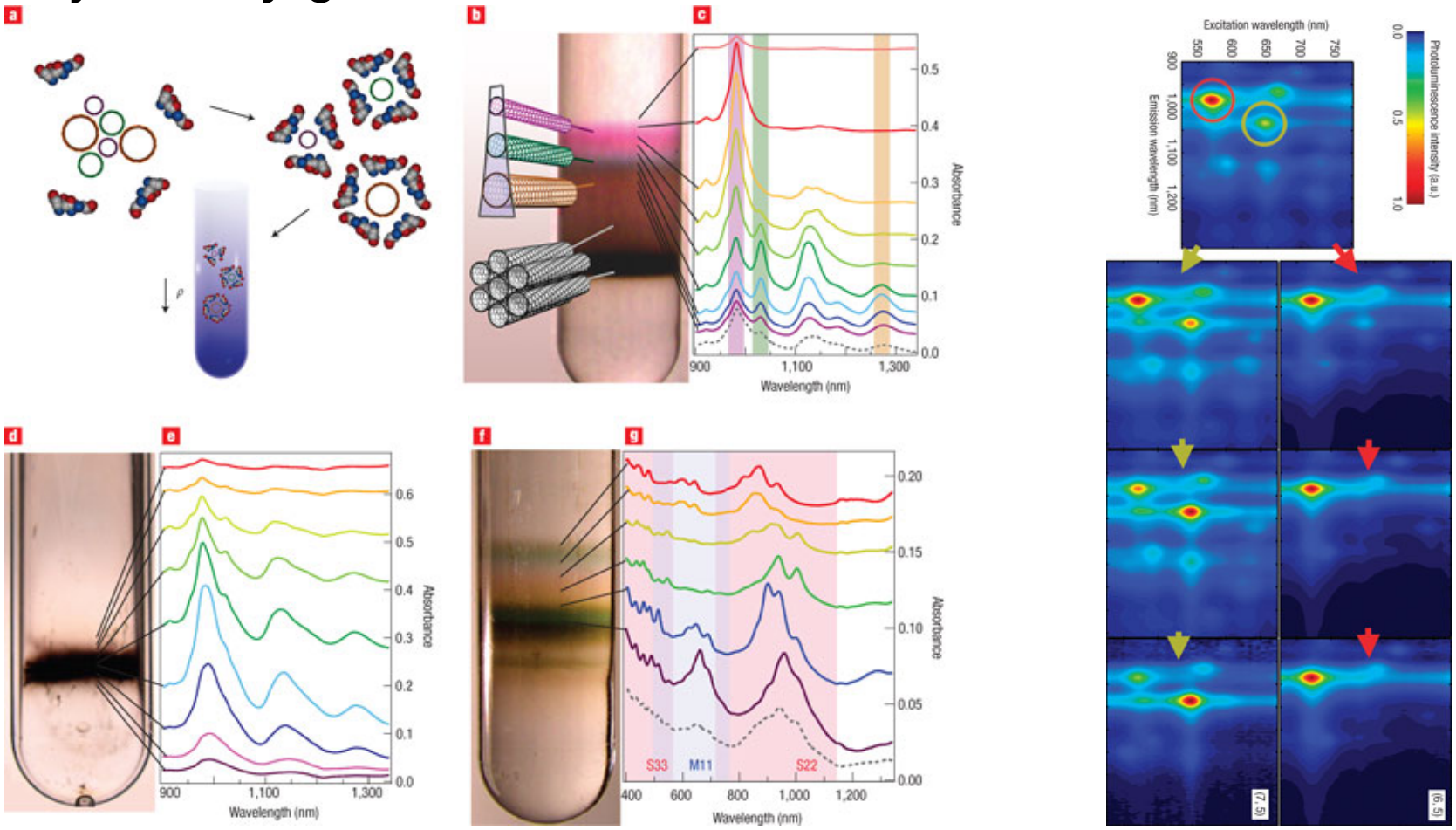


Huaping Liu et al., Nature Com, 2010

Placement strategies

- Single-chirality separation of single-wall carbon nanotubes by density gradient

Michael S. Arnold **et al., Nature Nano, 2006**



Placement strategies

- DNA sequence for structure-specific separation of carbon nanotubes.

X. M. Tu et al., Nature 2009

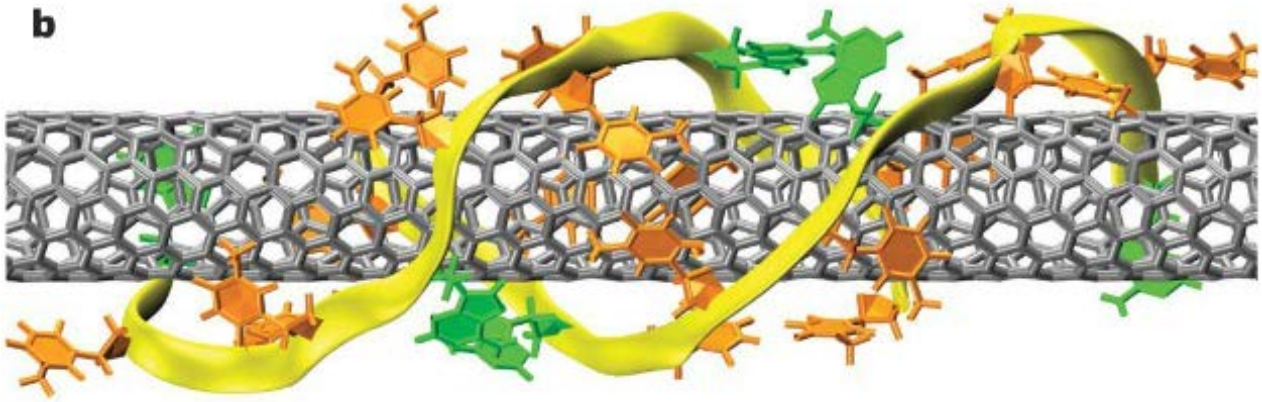


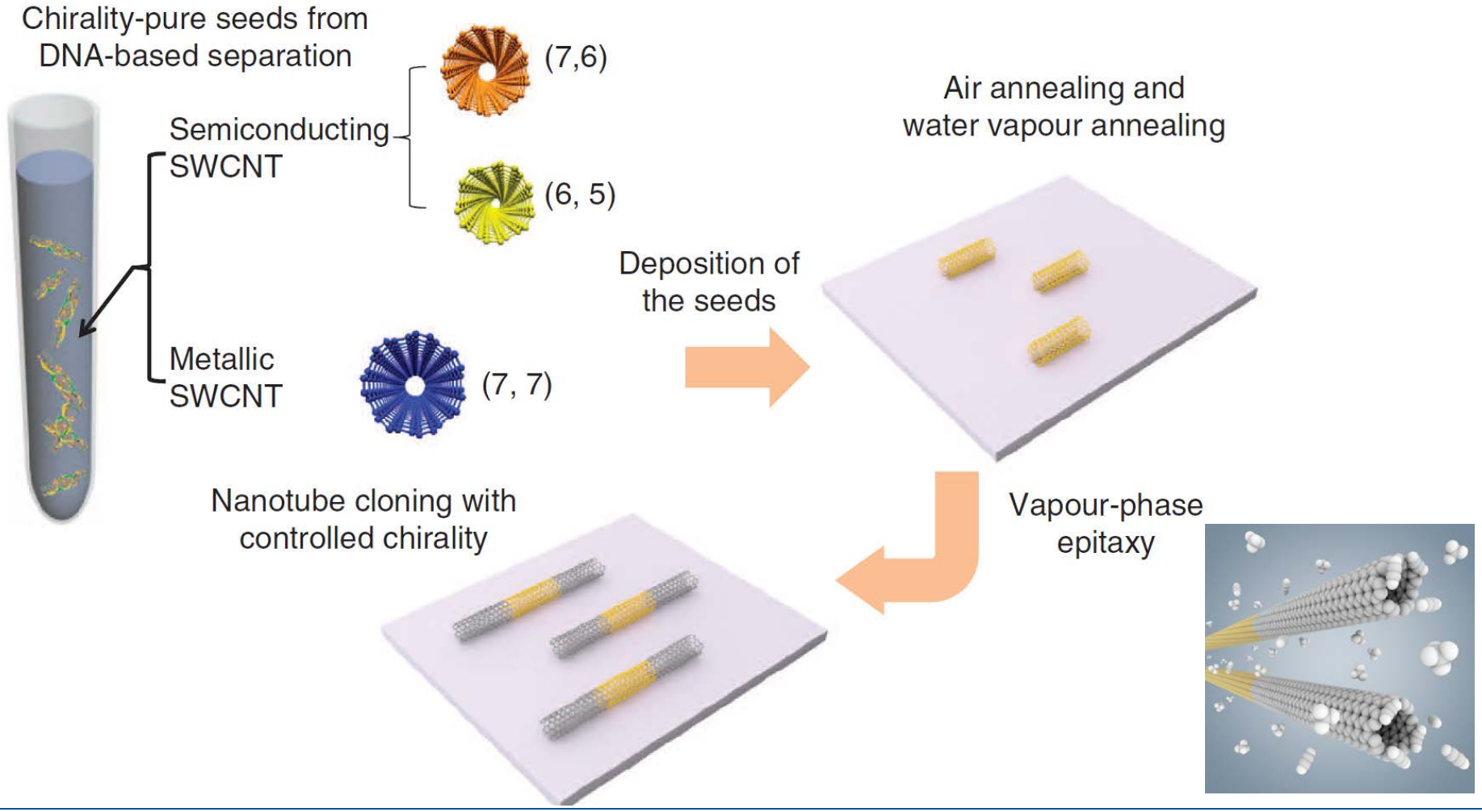
Table 2 | Experimental conditions and quantification

Chirality (*n*,*m*)	Sequence	Dispersion solution*	Incubation period†	Yield‡ (μg per 100 μg)	Purity§ (%)
(9,1)	$(TCC)_{10}$	0.1 M NaCl	None	0.1	80
(8,3)	$(TTA)_3TTGTT$	0.1 M NaCl	1 day	0.1	70
(6,5)	$(TAT)_4$	0.1 M NaCl	None	0.5	90
(7,5)	$(ATT)_4AT$	0.1 M NaCl	None	0.2	90
(10,2)	$(TATT)_2TAT$	0.1 M NaCl	None	0.1	90
(8,4)	$(ATTT)_3$	0.1 M NaCl	None	0.3	90
(9,4)	$(GTC)_2GT$	0.1 M sodium acetate pH 4.5	2 days	0.5	60
(7,6)	$(GTT)_3G$	0.1 M NaCl	None	0.4	90
(8,6)	$(GT)_6$	0.1 M NaCl	1 day	0.8	90
(9,5)	$(TGTT)_2TGT$	0.1 M NaCl, 10% glycerol	None	0.3	70
(10,5)	$(TTTA)_3T$	0.1 M sodium acetate pH 4.5	2 days	0.5	90
(8,7)	$(CCG)_2CC$	0.1 M NaCl, 10% glycerol	None	0.4	80

Placement strategies

Jia Liu et al., Nature Com 2012

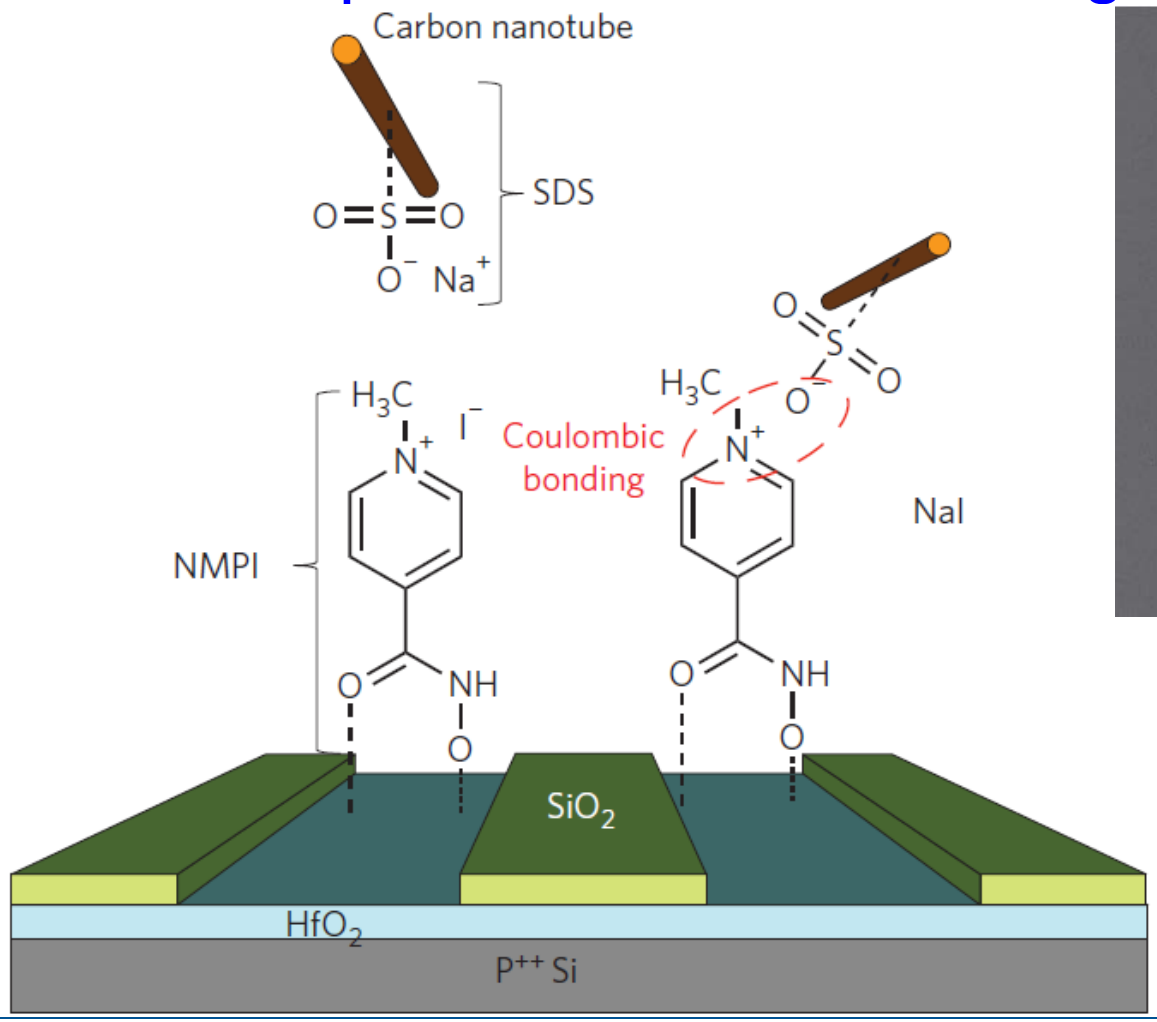
❑ Cloning of a specific chirality

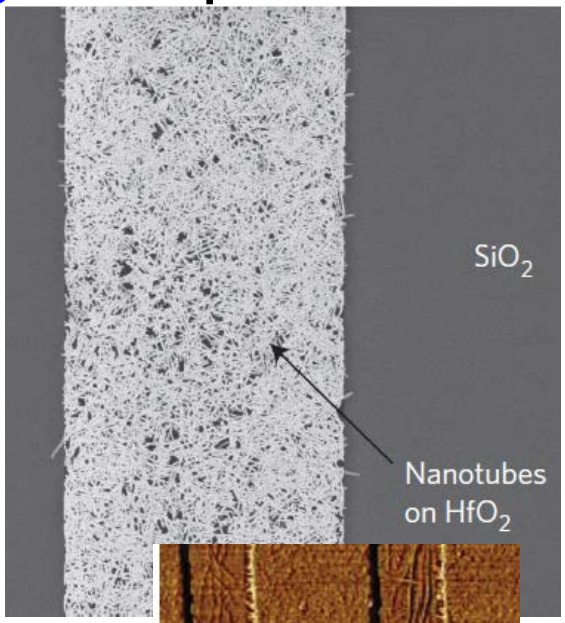


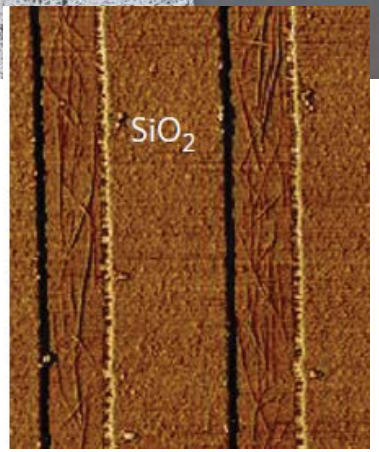
Placement strategies

Hongsik Park et al., Nature Nano 2012

- Site specific selective binding to deposit nanotubes



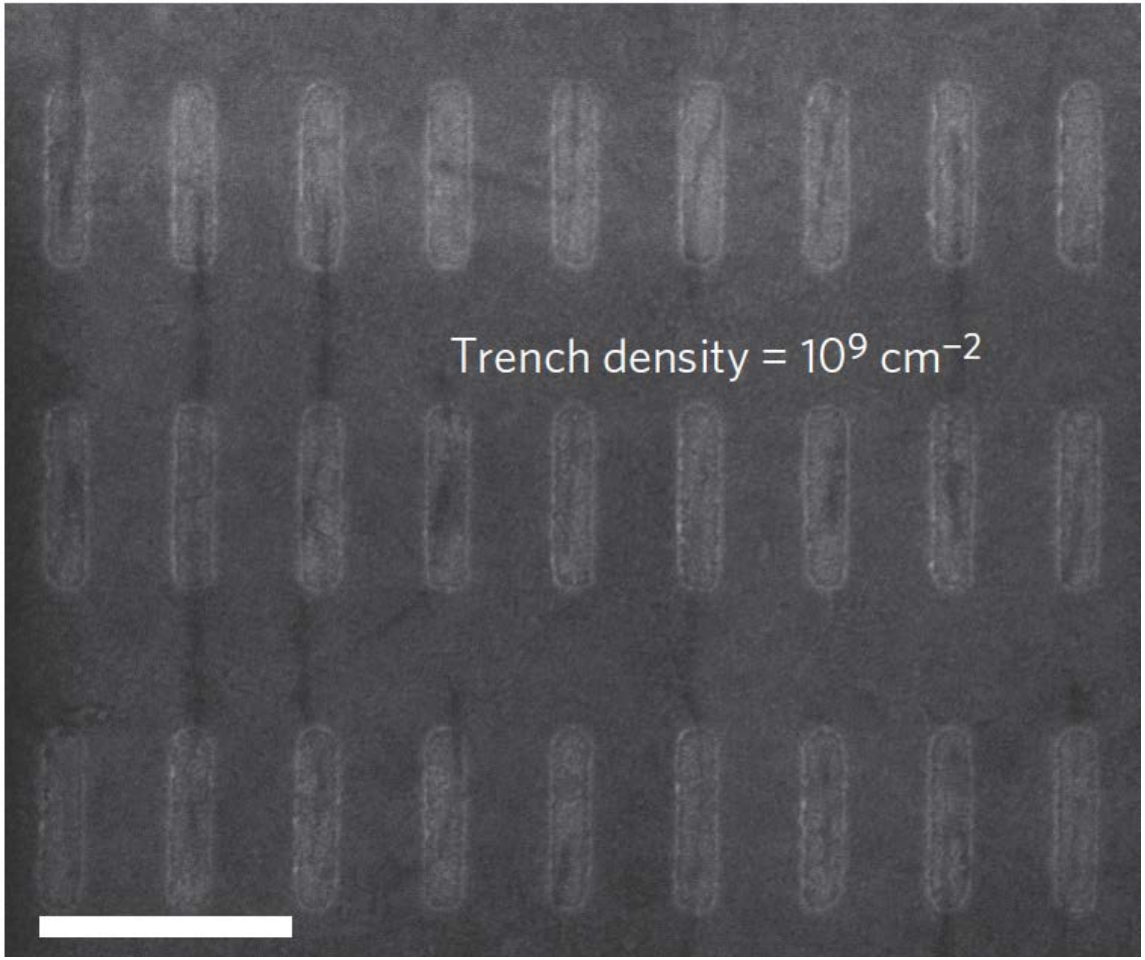




Placement strategies

Hongsik Park et al., Nature Nano 2012

- Site specific selective binding to deposit nanotubes

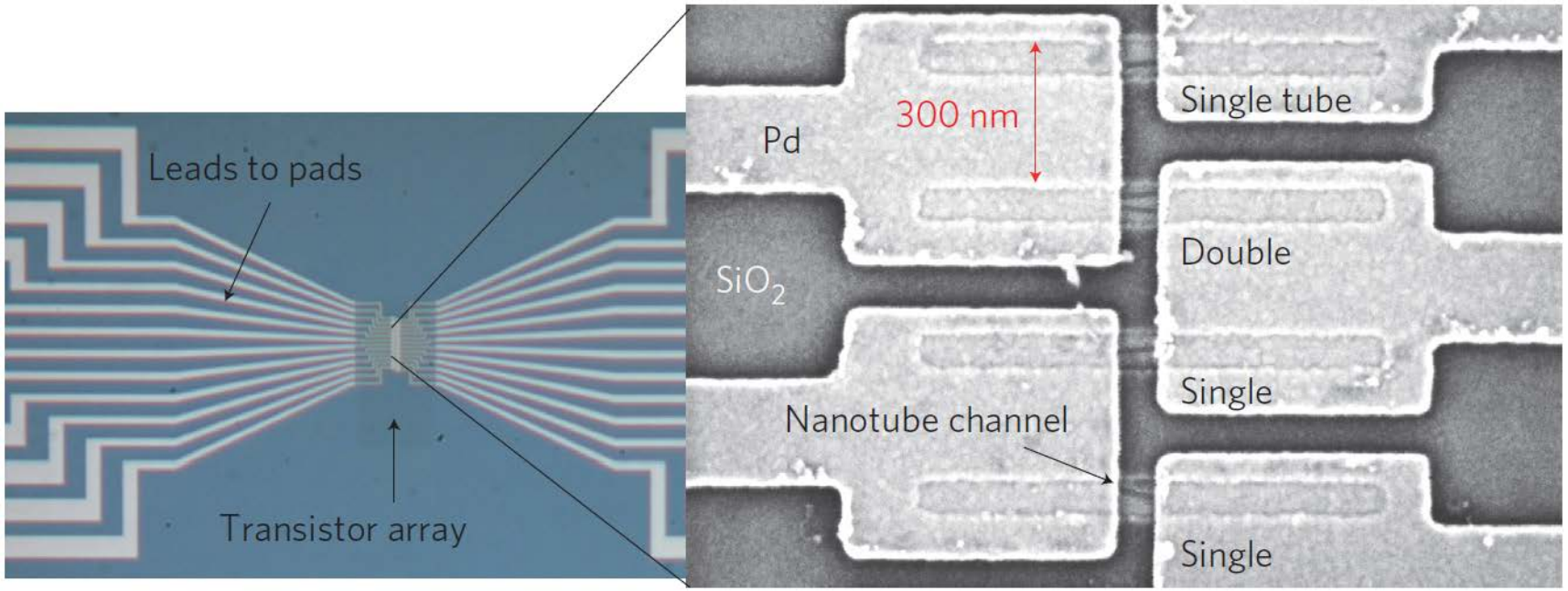


- 200 nm pitch in the x-direction
- 500 nm pitch in the y- direction
- 10^9 sites/cm^2 density (scale bar, 400 nm).
- precise placement in two dimensions
- 90% of the trenches contain at least one nanotube

Placement strategies

Hongsik Park et al., Nature Nano 2012

- Fabricate devices at the CNT-filled trenches

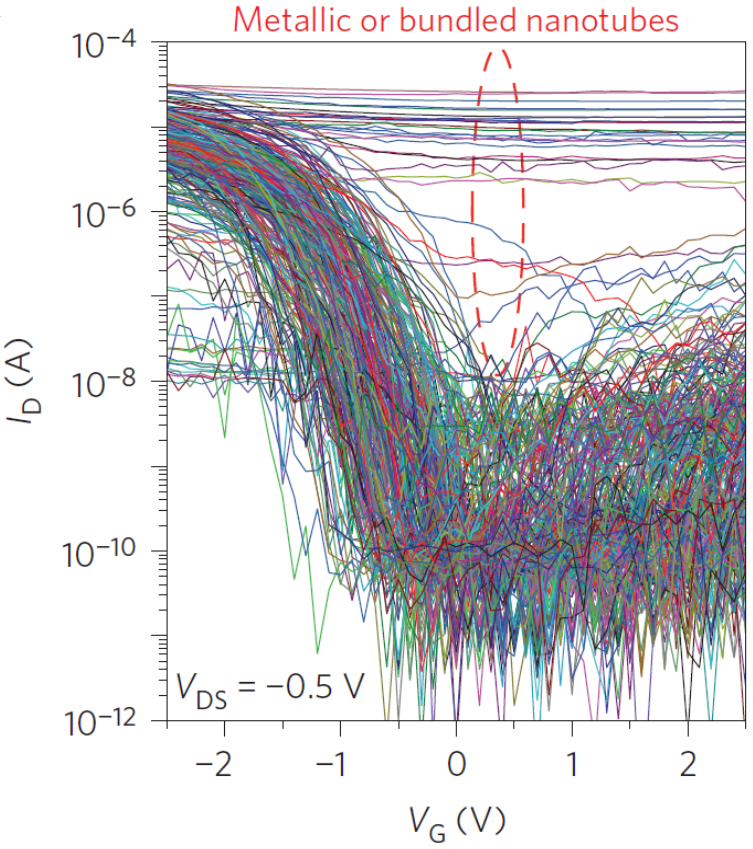


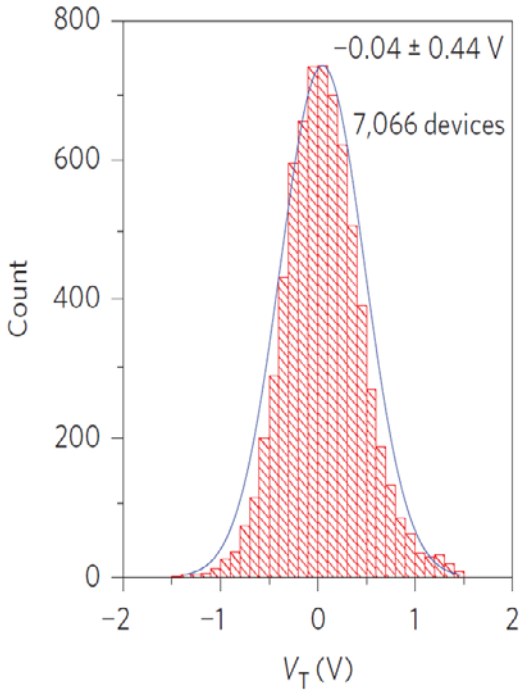
- More than 10,000 devices have been fabricated over the pre-patterned trenches with CNT-selfassembly by ion-exchange reaction

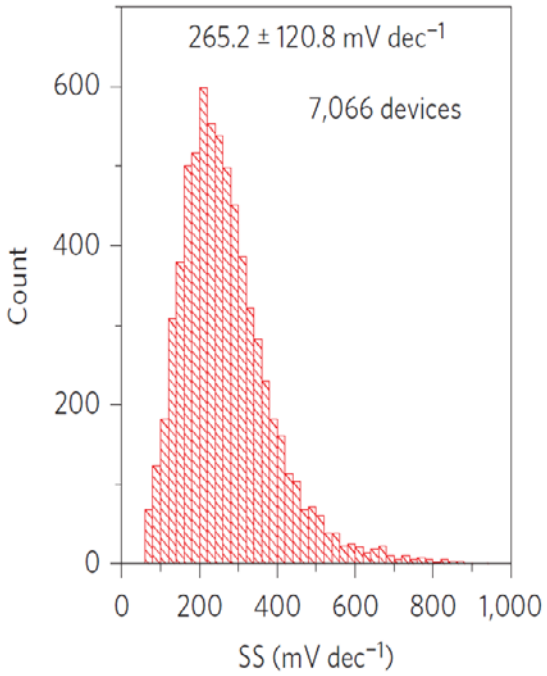
Placement strategies

Hongsik Park et al., Nature Nano 2012

- Evaluation of more than 10,000 CNT devices





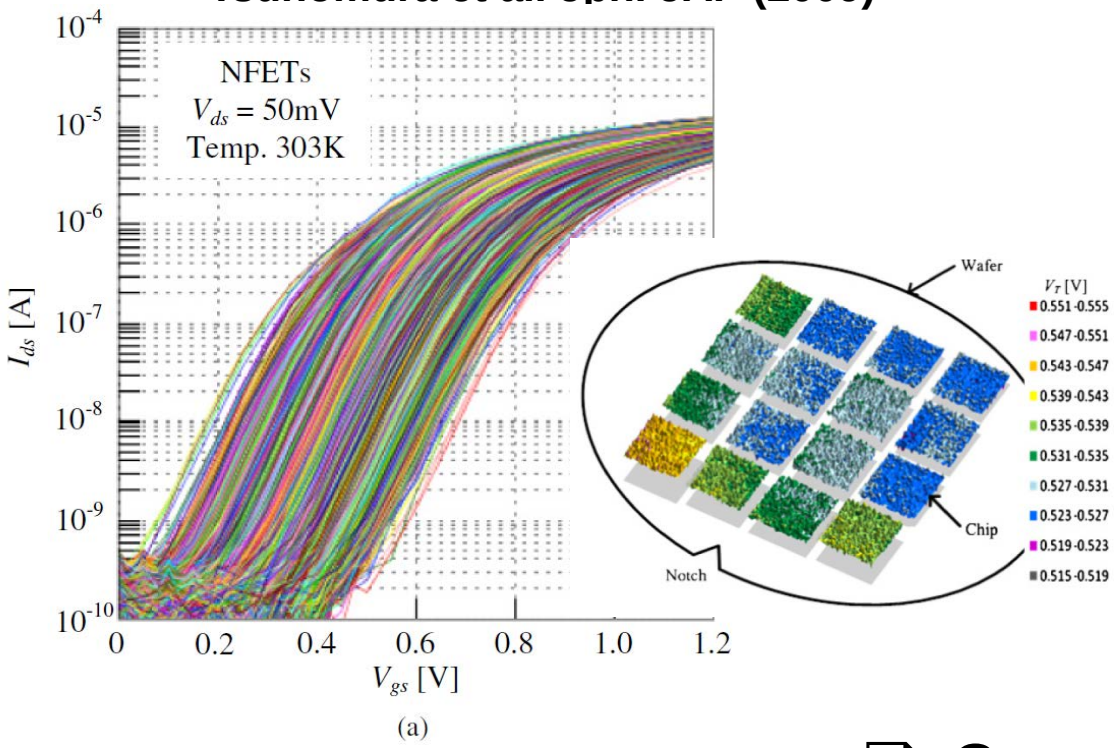


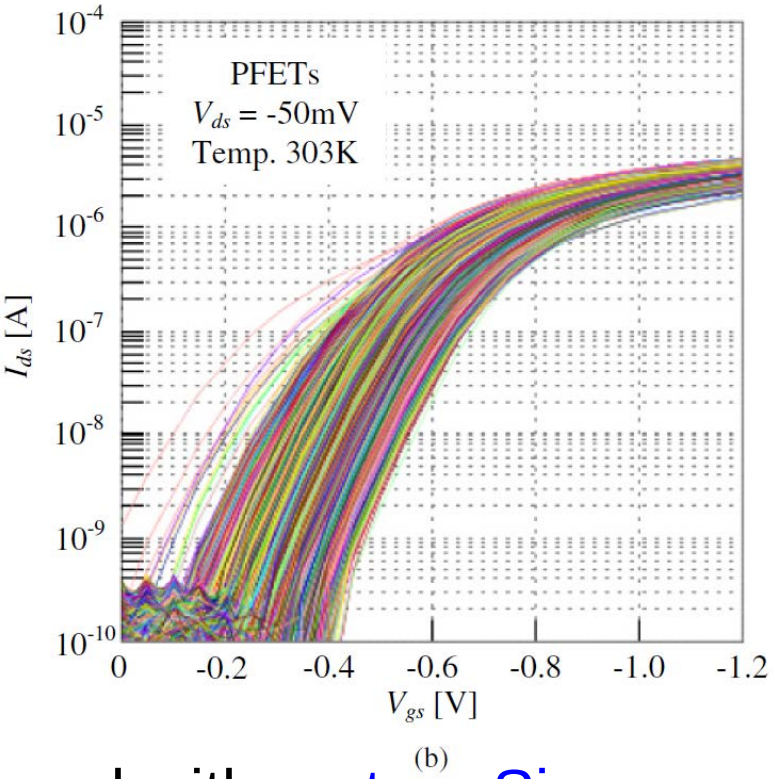
- This is an amazing result – given that 2 people have worked on the topic for a couple of month

Just compare – for a moment - with Si

- Evaluation of more than **1 million CMOS** FETs

Tsunomura et al. Jpn. JAP (2009)





- gate length is 60 nm and
- gate width is 140 nm

- Compared with mature Si-technology - CNT assembly is not too bad

Summary

- Opportunity window for alternative channel materials is closing
- Performance-wise carbon nanotube devices outperform any alternative
- Huge gap for industrial integration exists
- A possible roadmap exists based on self-assembly
- The low-hanging fruits for nanotube device research are gone
- What remains is hard work to make it happen – not ideally suited for academia