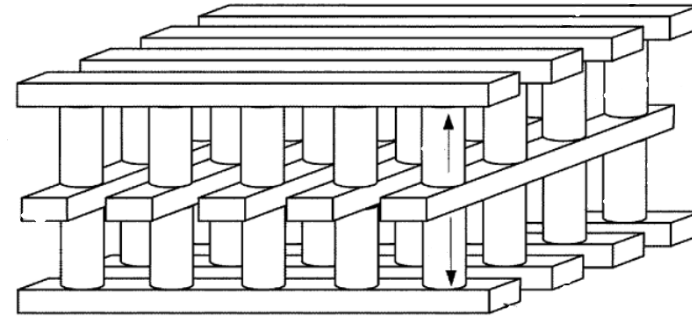
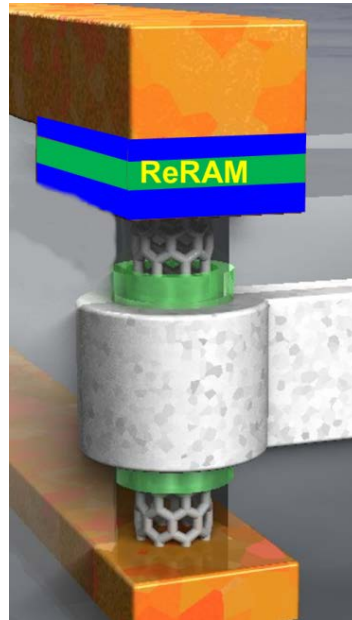
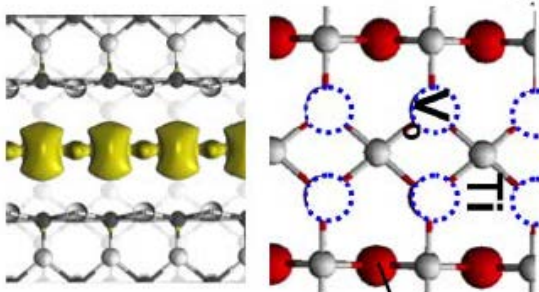


# Material and design aspects of ReRAM technology

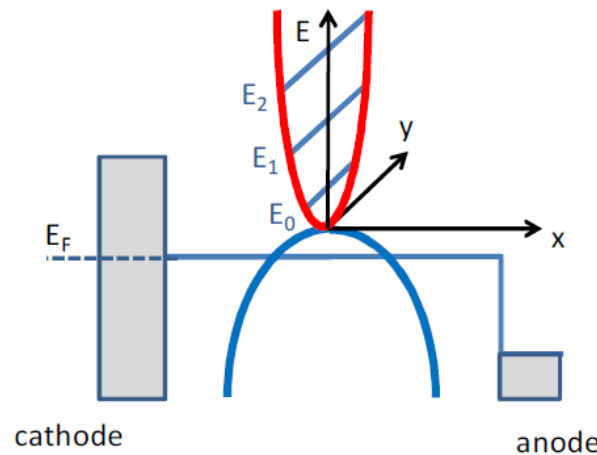
E1 (TiN)
E1 (n+ Si)
RSL1 (MeOx)
Cap1 (TiOx)
IL (TiN)
IL (n+ Si)
RSL2 (MeOx)
Cap2 (TiOx)
E2 (TiN)



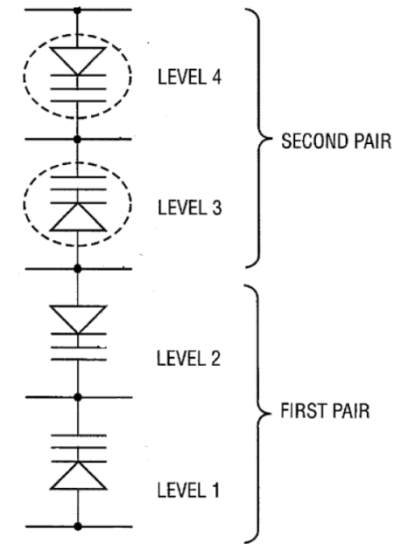
Kreupl et al., US 2011/0310654 A1



Kamya et al. IEDM 2012



R Degraeve et al. IEDM 2010



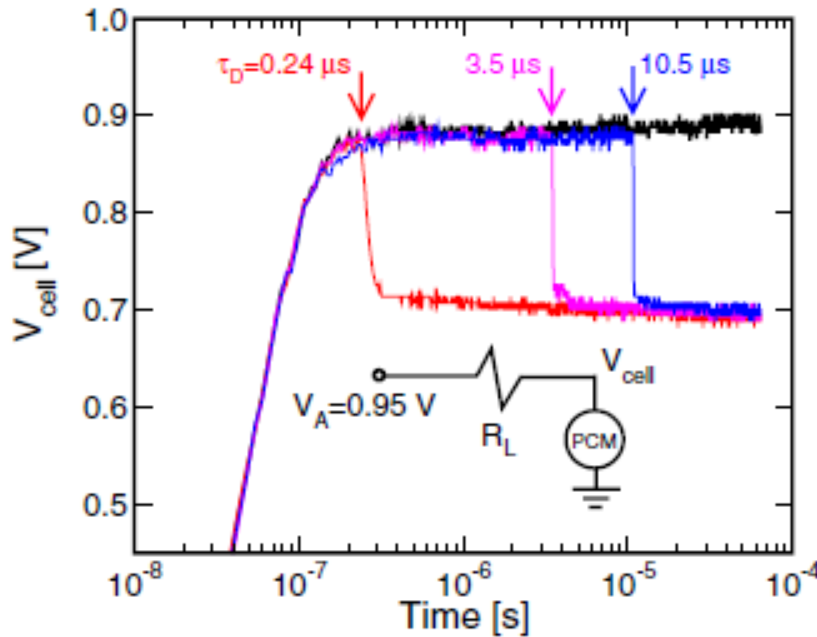
# Outline

- ReRAM memory technologies (why there is no Memristor)
- The cell and its electromagnetic environment
- DC-I(V) sweeps don't tell you the truth (dynamic currents)
- Understanding current overshoot
- Where is the resistor in the cell?
- How to operate at low currents?
- In-cell resistor
- Contact resistor
- Active Feedback Cell (AFC)
- Summary

# ReRAM Memory Technologies

## - why there is no Memristor -

- PCRAM, CBRAM, ReRAM (MeOx) are **threshold switches**

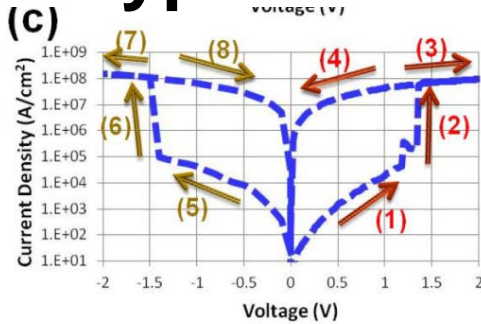


Lacaíta et al, IEDM 08

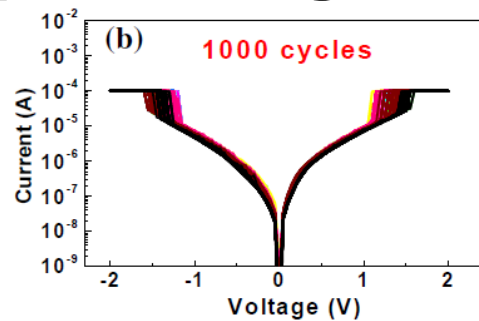
$$I_{Cell} = \frac{V_{appl} - V_{Cell}}{R_{Bitline}} - C \frac{dV_{Cell}}{dt}$$

- close to  $V_{Threshold}$  it can take very long, so you need to operate at  $V_{appl} > V_{Threshold}$
- This makes  $dV_{cell}/dt$  big, as time  $dt$  is  $\sim 100$  ps

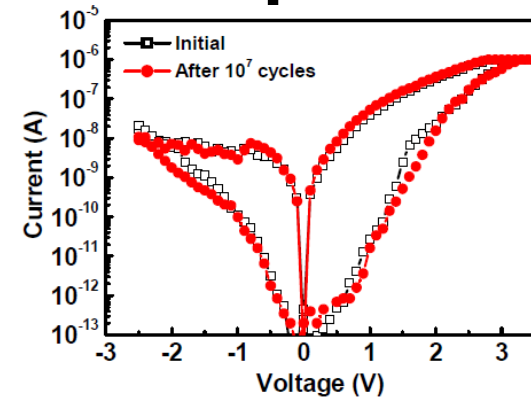
# Typical DC I(V) showing low current operation



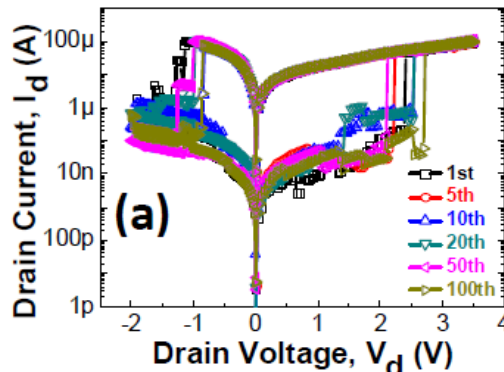
ChiaHua Hoet et al. IEDM 2012



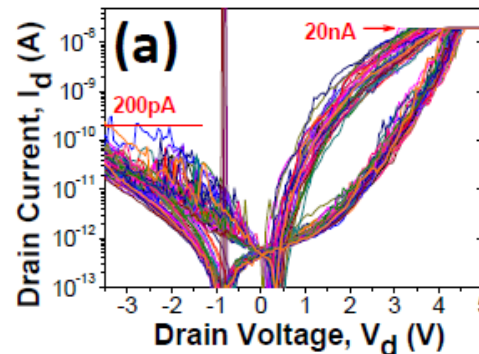
Myoung-Jae Lee et al. IEDM 2012



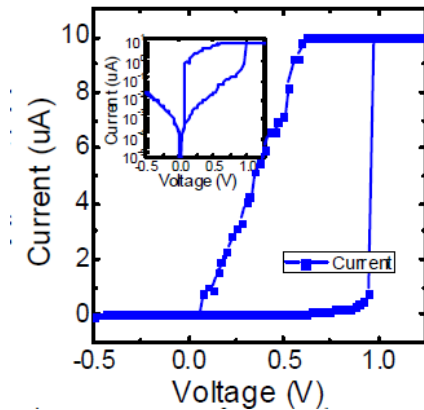
Seong-Geon Park et al. IEDM 2012



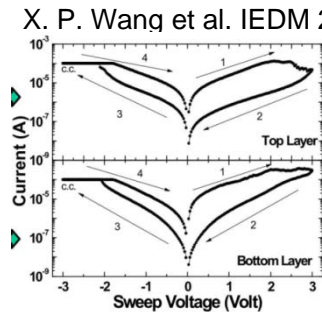
X. P. Wang et al. IEDM 2012



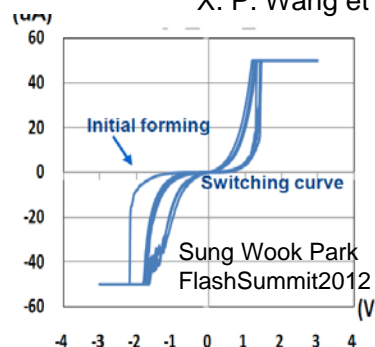
X. P. Wang et al. IEDM 2012



F.M. Lee et al. I VLSI 2012



W.C. Chien et al VLSI 2012

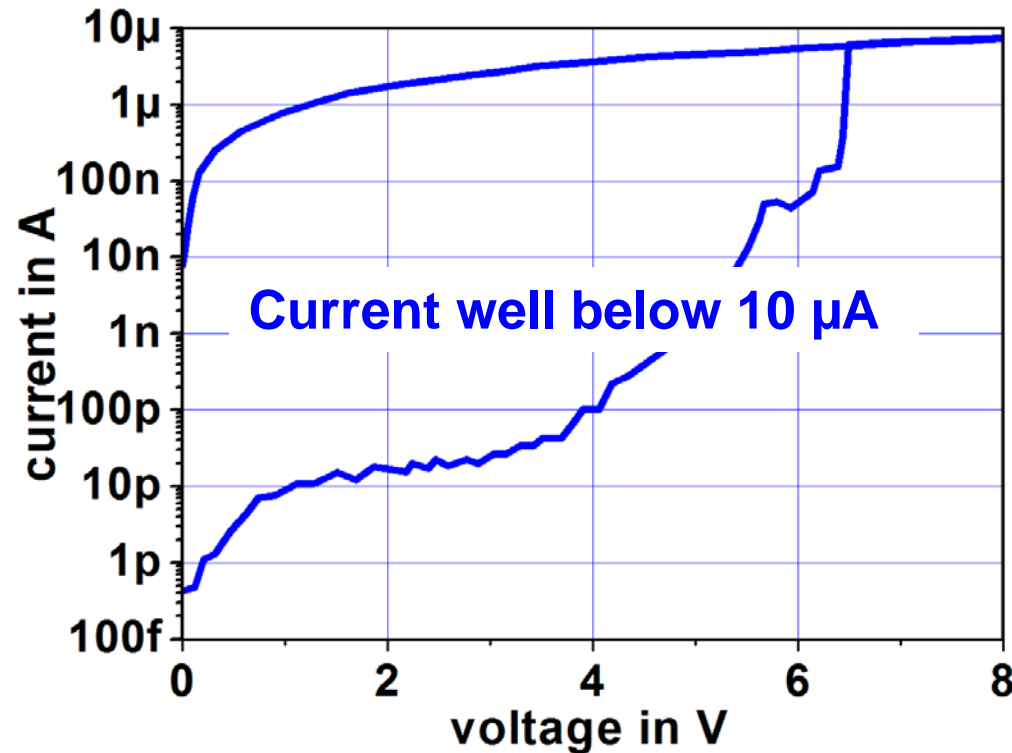


Sung Wook Park  
FlashSummit2012

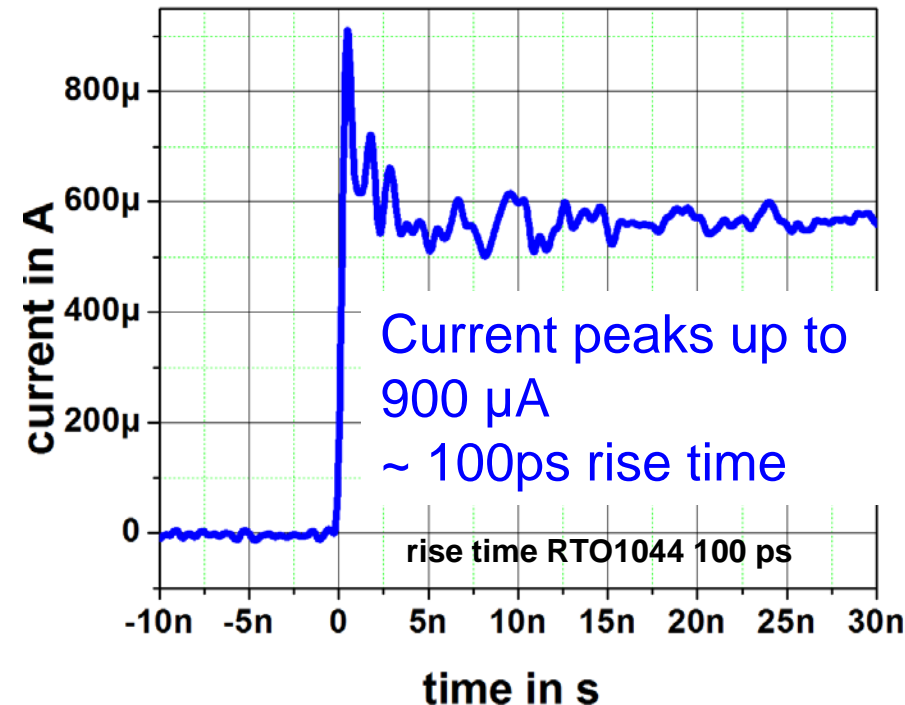
Is this low current true?  
Depends on measurement setup!

# Dynamic currents will be much higher

This is what SMU reads

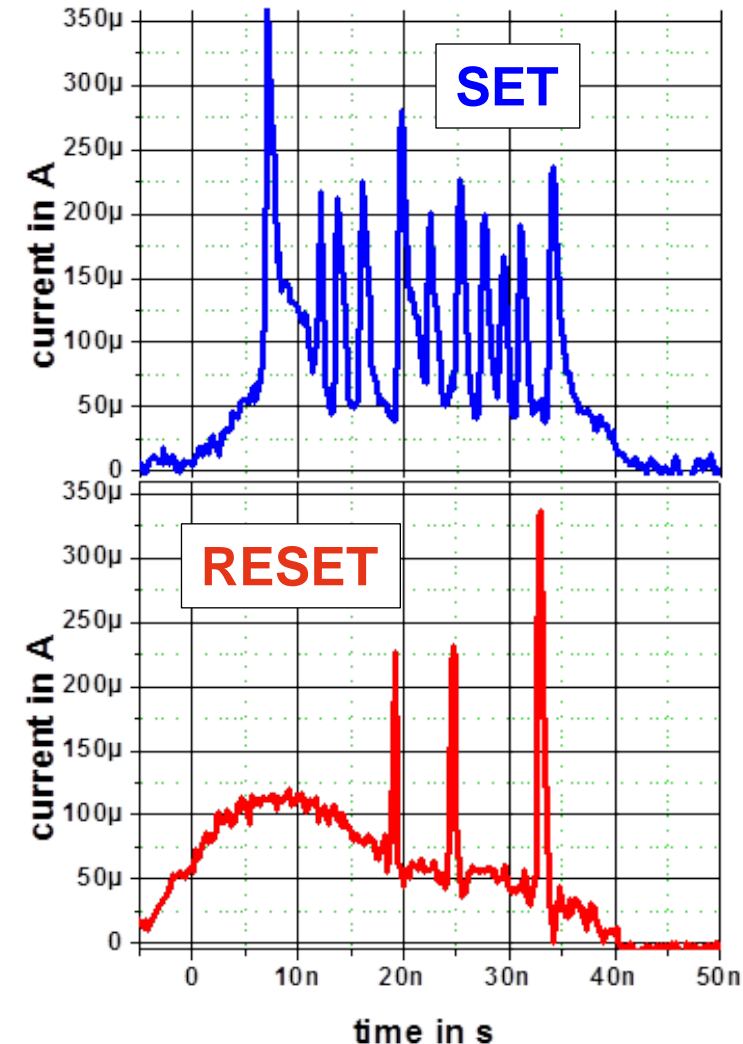


This is what goes thru the cell



Most published data give  $I(V)$  sweeps as evidence for low current.  $I(V)$  sweeps don't tell too much about the dynamic currents!

# Dynamic currents in pulse mode



- High current peaks from capacitance
- The filamentary nature gives very high local temperature – current density!

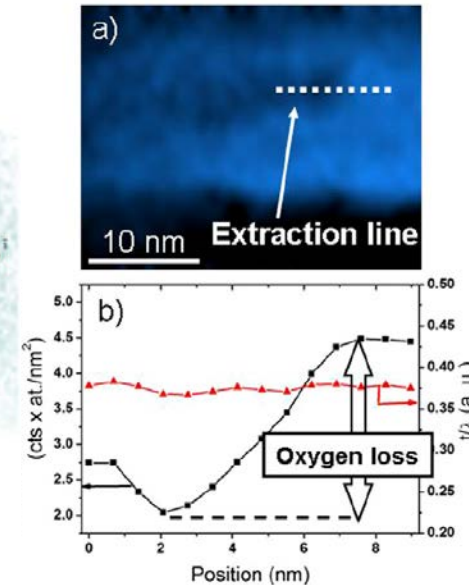
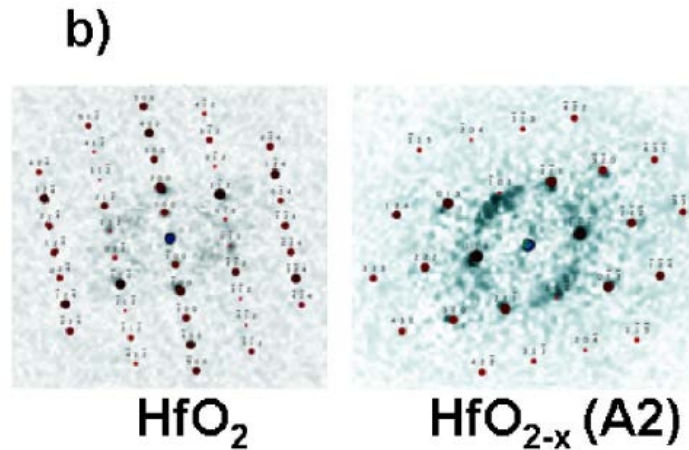
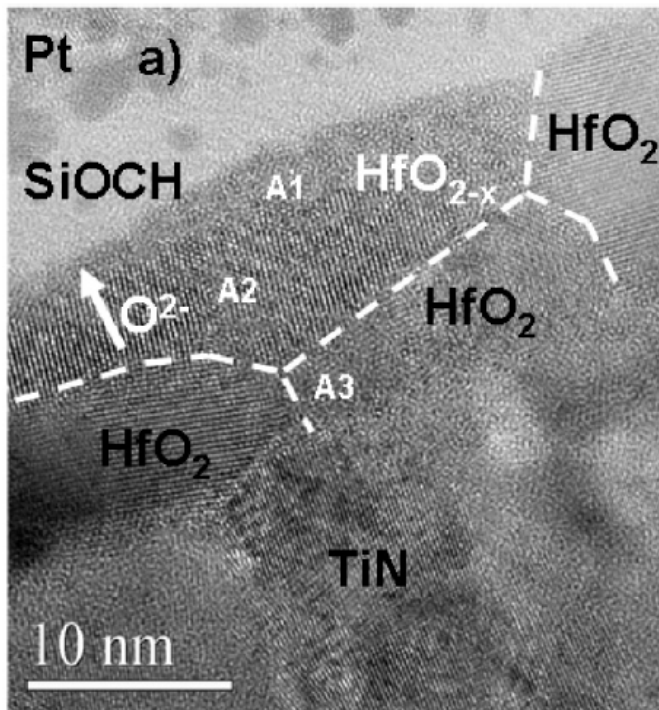
$$\square T_{\text{filament}} = T_0 + j^2 \rho C \quad \text{for } t < 1 \text{ ns}$$

$$\square T_{\text{filament}} = T_0 + j^2 \rho \frac{L^2}{8Ck_{th}} \quad \text{for } t > 1 \text{ ns}$$

- High T creates phase transformation, alloying, diffusion, electromigration etc.
- Key question:  
 Will the material/cell switch at all if cap-discharge is neglectable – as in 1x nodes?  
 Will it be stable?

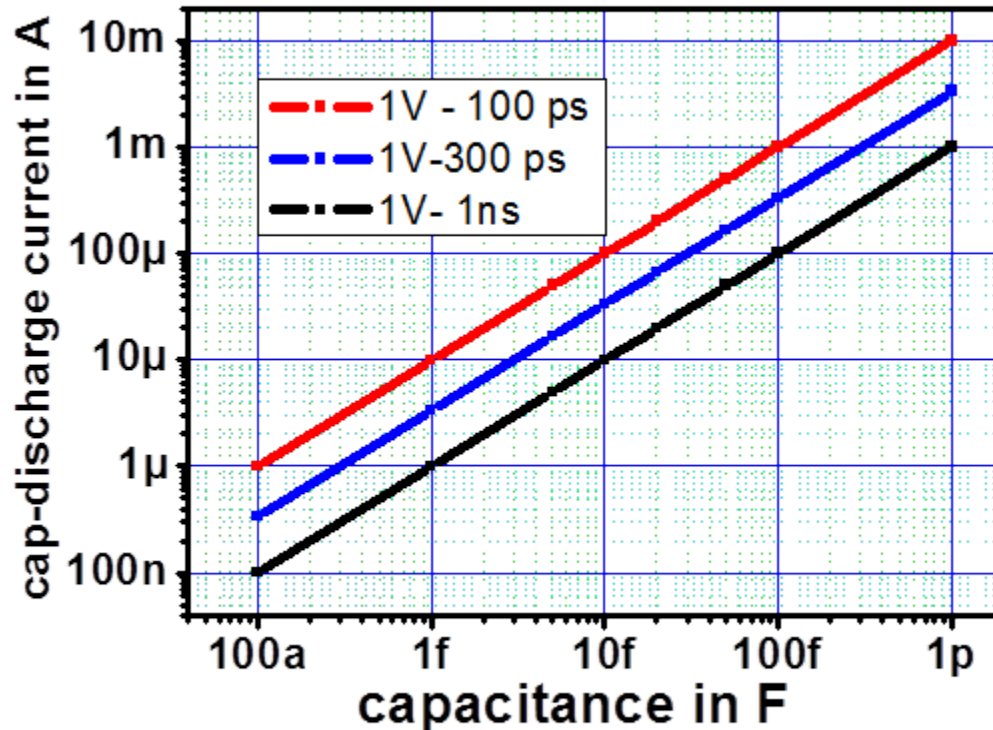


# Amorphization and O-loss attributed to high current density



- ❑ Extensive analysis of **nanofilaments** in HfO<sub>2</sub> by Calka et al. (2013) shows:
  - ❑ **High T** creates amorphization, **diffusion and movement of oxygen**
  - ❑ Accumulation of oxygen at the Pt anode
  - ❑ Crystallization of the TiN bottom electrode
- ❑ Will this **mechanism work** if current is **reduced** ?

# Typical cap-discharge current



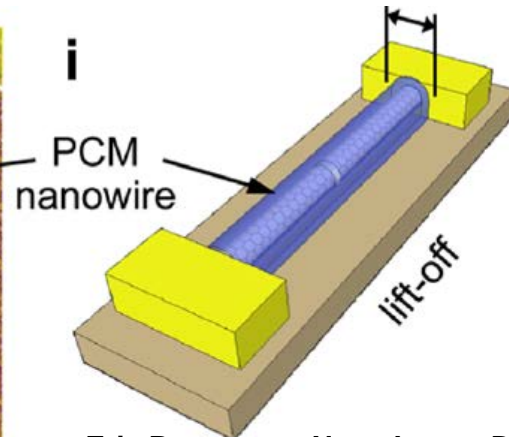
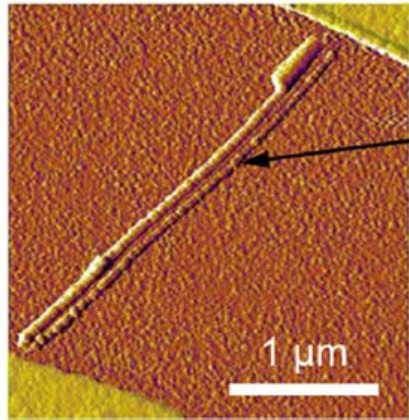
- Speed is within rise time of the scopes
- Relevant capacitance is within a sphere of  $r = t \cdot v_{prop.} < 100ps \cdot v_{prop.}$  (Wahlgren – horizon picture)

- My experience: cell  $R_{ON}$  is defined by first (forming)  $C \cdot dV/dt$
- That's the reason why most data have the same low  $R_{ON}$ , ( $< \sim 20$  kOhm) independent of the used material or stack

M. Terai et al., EDL 2010

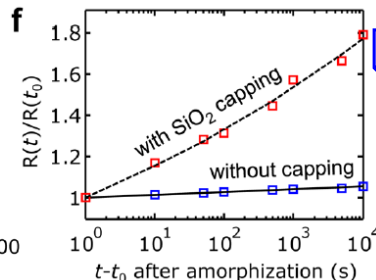
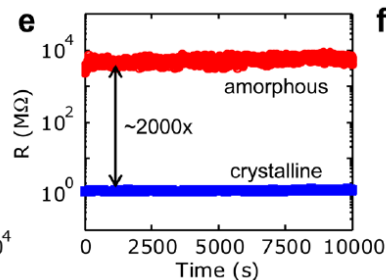
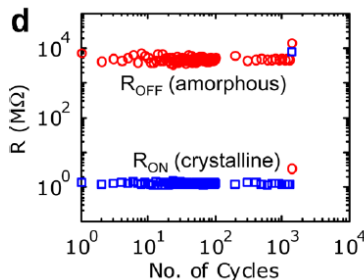
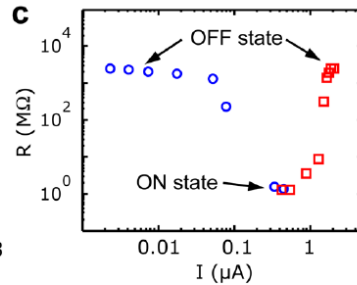
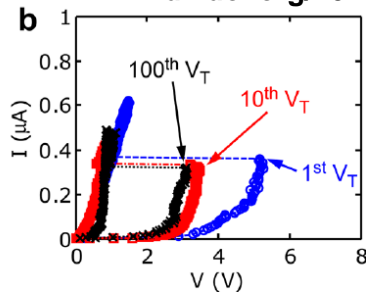
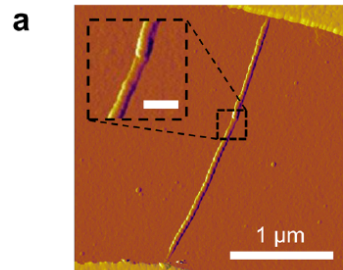


# 0.1 $\mu\text{A}$ set, $\sim 1.6 \mu\text{A}$ reset by capacitance reduction

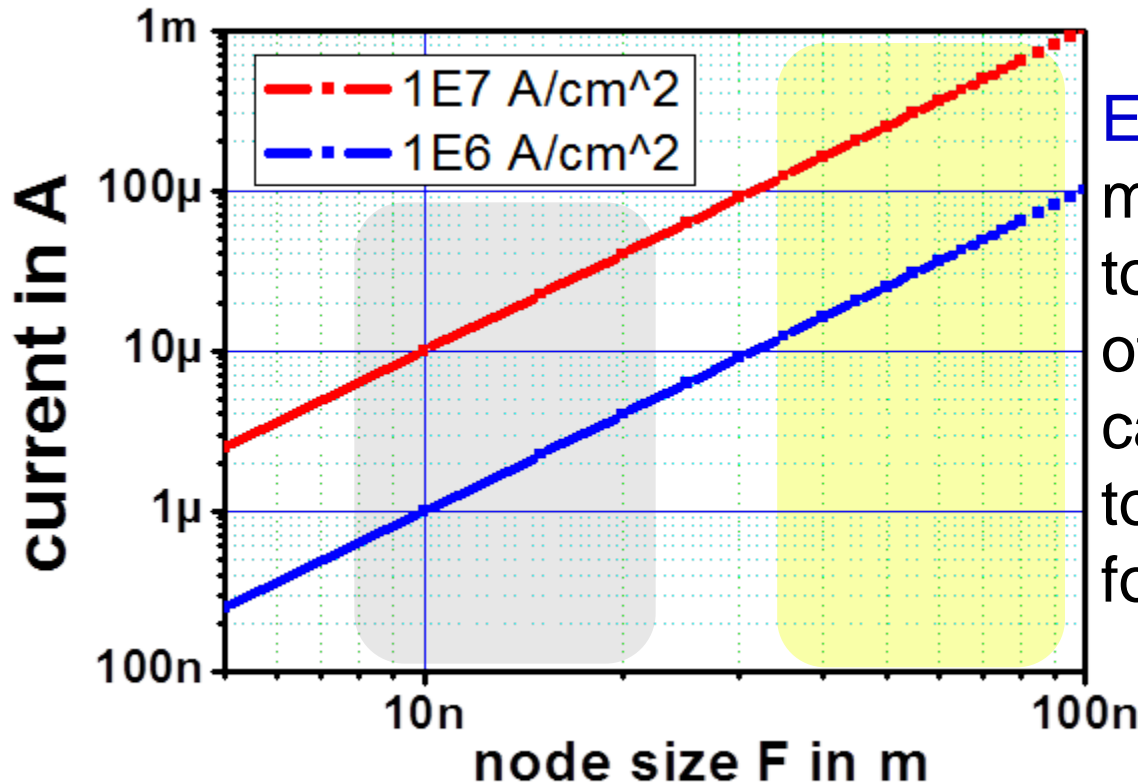


Eric Pop group, Nano Letter, Dec. 2012  
[dx.doi.org/10.1021/nl3038097](https://doi.org/10.1021/nl3038097)

- ❑ Local capacitance reduction by using CNT contacts
- ❑ The resistance of the CNT (contact and quantum) shields the external capacitance
- ❑ The small contact area gives very small local capacitance
- ❑ Low current switching possible in a threshold-voltage controlled cell



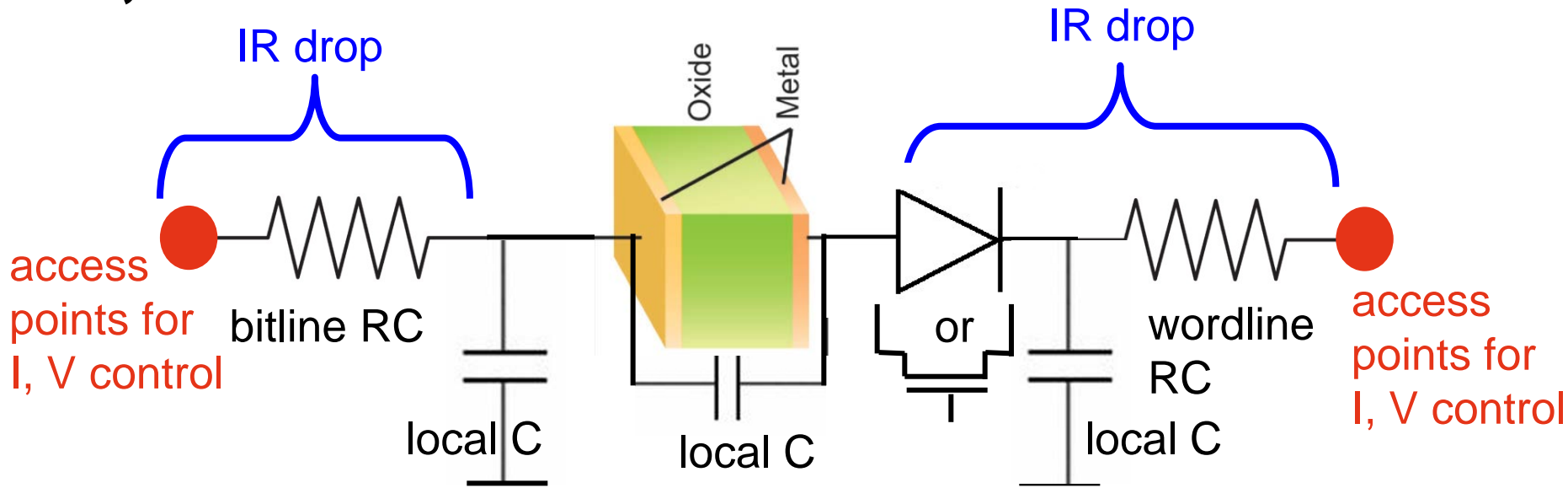
# Typical currents and related current densities



E-field driven ion movement needs to flow the same amount of current like in the cap discharge event, to create the same field for bipolar reset.

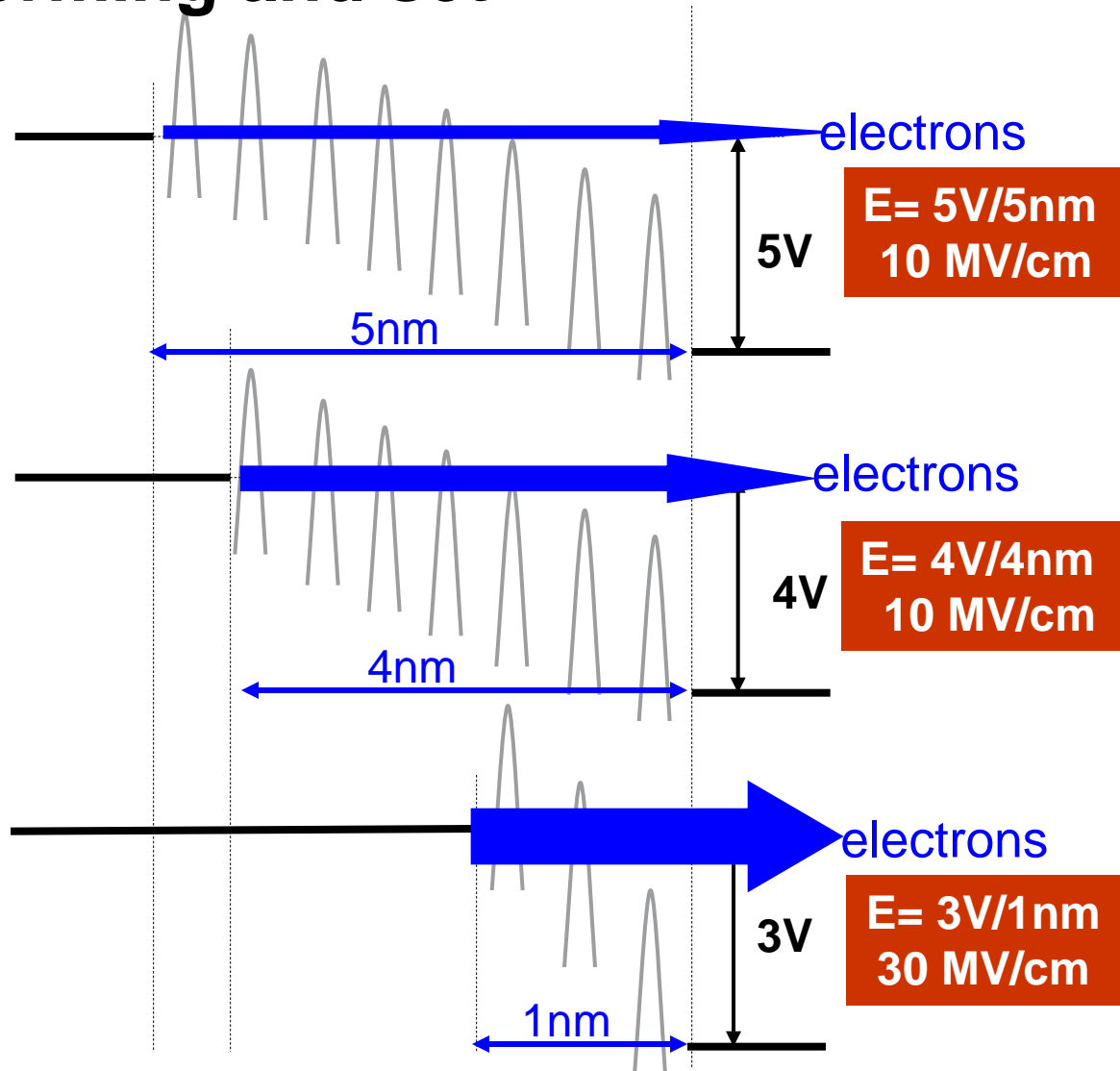
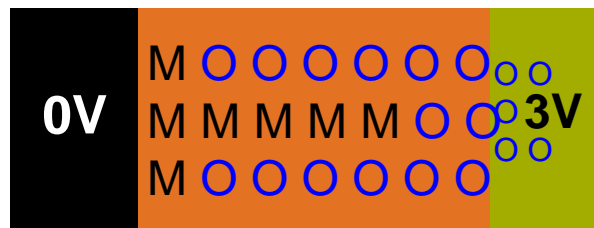
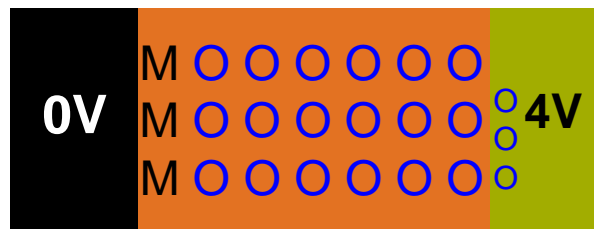
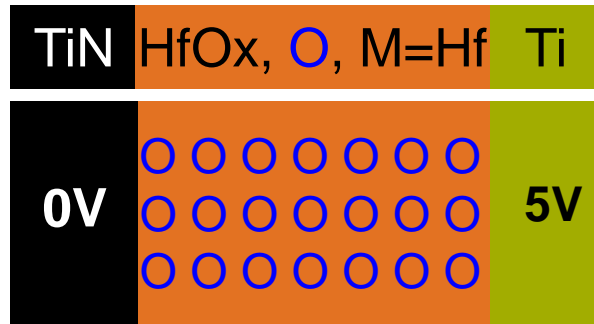
- ❑ At advanced nodes, current density is close to the reliability limit of most conductors and devices
- ❑ By  $j^2 \rho$ , huge temperatures are induced, pulses should be as short as possible to limit this energy imprint

# Bit-, word-line and device can't limit C-current

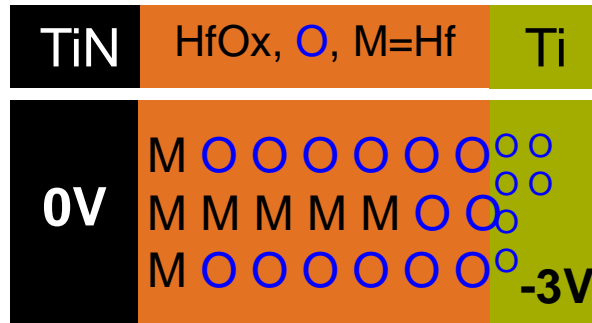


- ❑ Diode/FET or bit/word-line **can** only **shield** on **long time** scales
- ❑ Overall **capacitive discharge** is given by **local capacitance** which scales with (isolated) feature size
- ❑ **Transistor** has contact and diffusion **capacitance**, **smoothes**  $I_{peak}$
- ❑ But for an **high density array**, bit/word-line **cap** is **fixed** and **high!**
- ❑ **Local cap** acts as "**battery**" providing **high current** density **peaks**

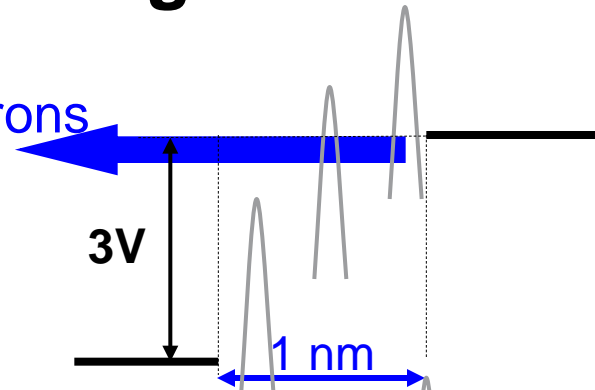
# Understanding forming and set



# Current transport during reset

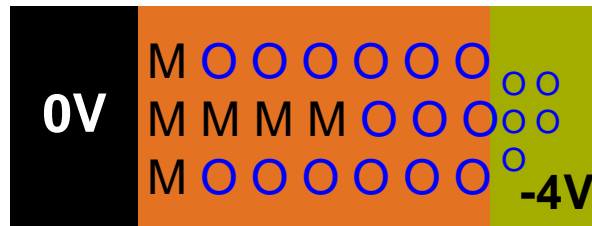


electrons

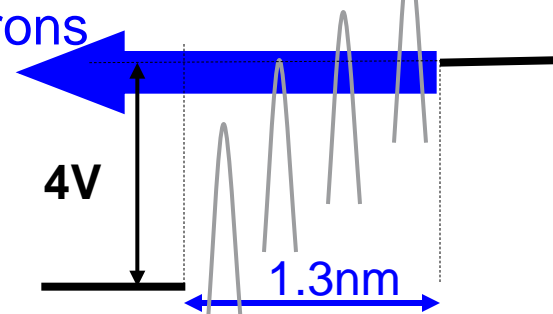


$$E = 3\text{V}/1\text{nm}$$

$$\sim 30 \text{ MV/cm}$$

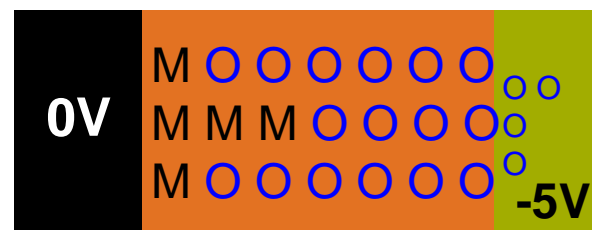


electrons

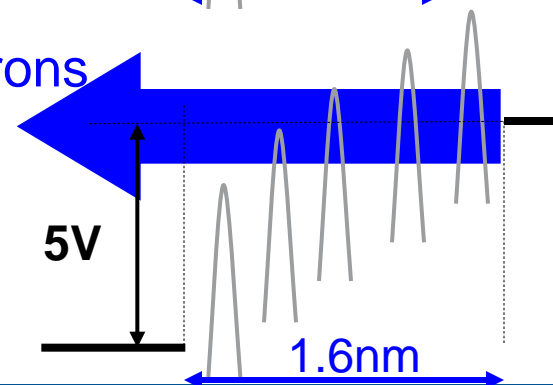


$$E = 4\text{V}/1.3\text{nm}$$

$$\sim 31 \text{ MV/cm}$$



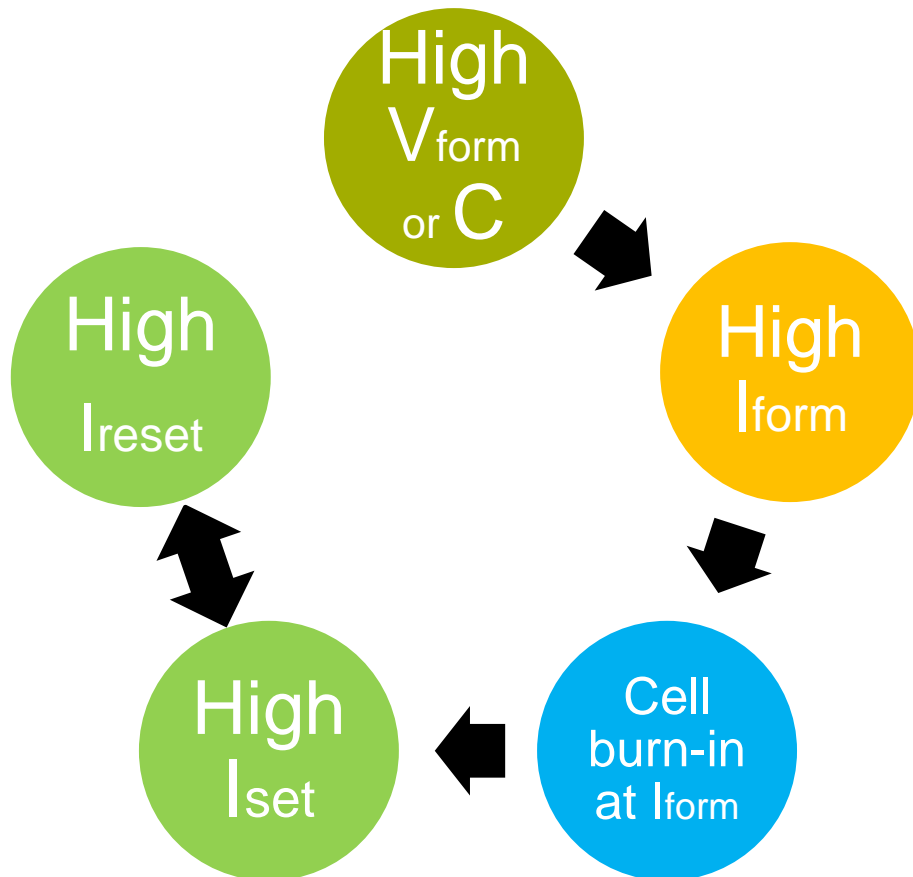
electrons



$$E = 5\text{V}/1.6\text{nm}$$

$$\sim 32 \text{ MV/cm}$$

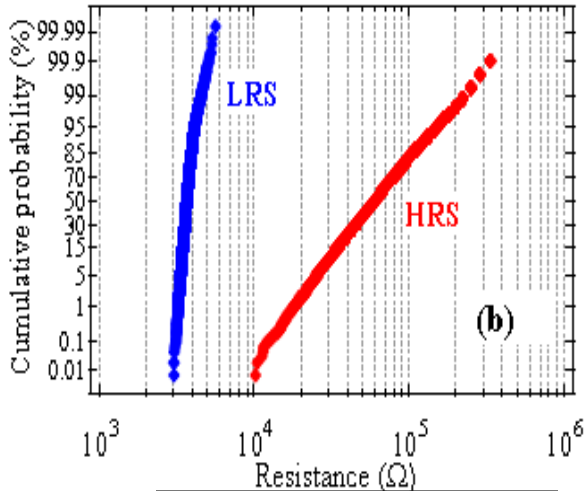
# Vicious interdependence



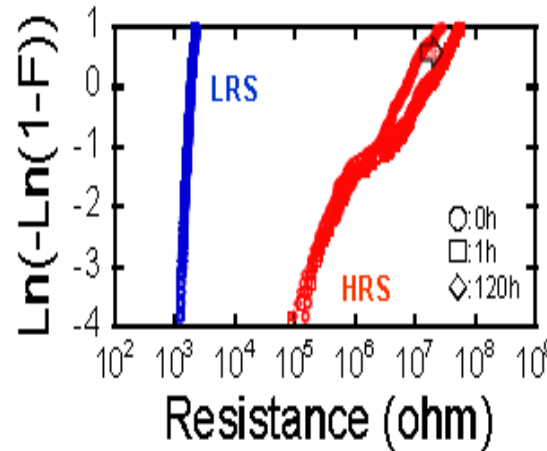
- ❑ High  $V_{form}$  and/or  $C$ :
  - ❑ cap-discharge
- ❑ High  $I_{form}$  :
  - ❑ transistor as current limiter?
  - ❑ diode as current limiter?
  - ❑ impact of pulse length?
- ❑ Low on-state resistance
  - ❑ fraction of one quantum channel
- ❑ best would be
  - ❑ low  $V_{form}$  and
  - ❑ smooth forming – no current peak
- ❑ Need built-in resistor!



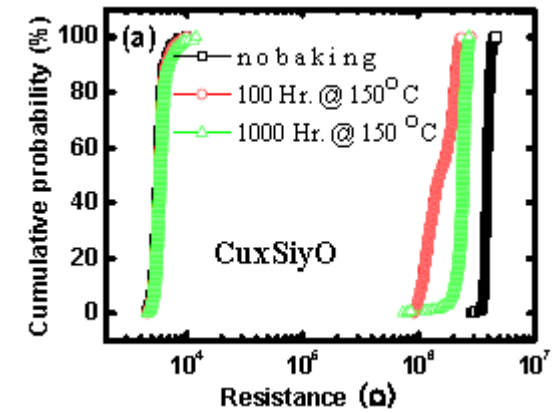
# Low on-resistance state - a consequence of C-discharge



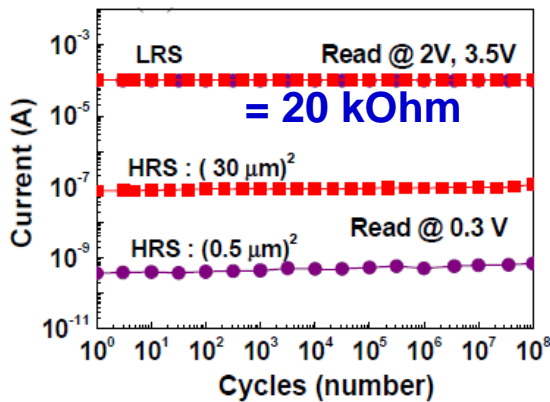
Panasonic, IEDM 2008



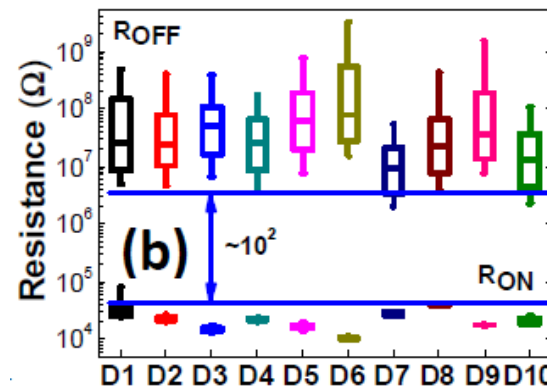
NEC, VLSI 2010



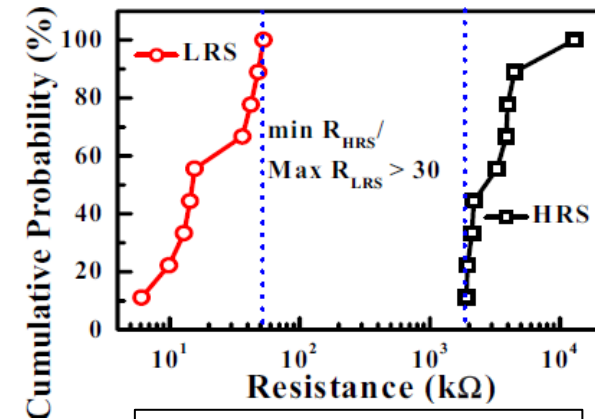
SMIC, VLSI 2010



Myoung-Jae Lee et al. IEDM 2012

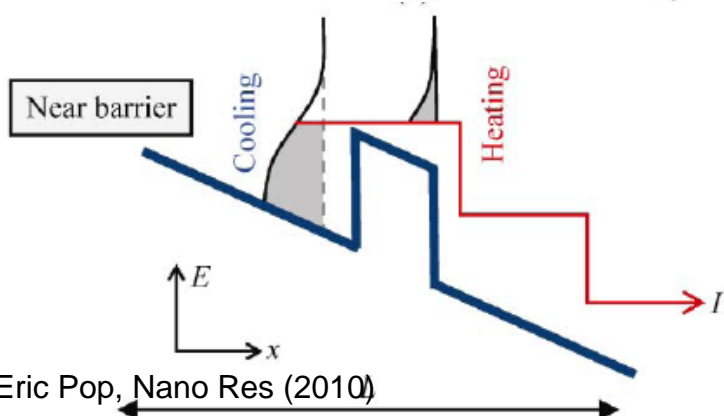
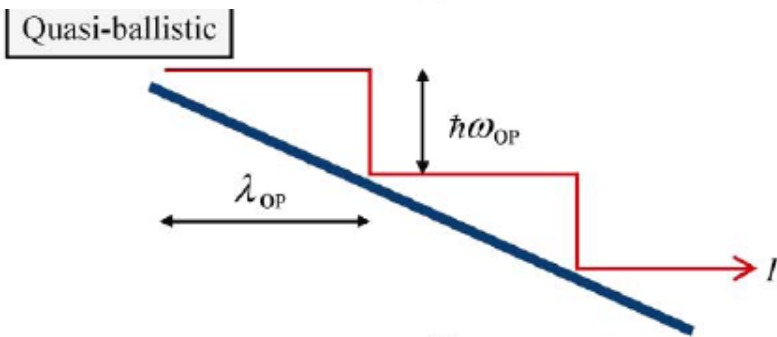
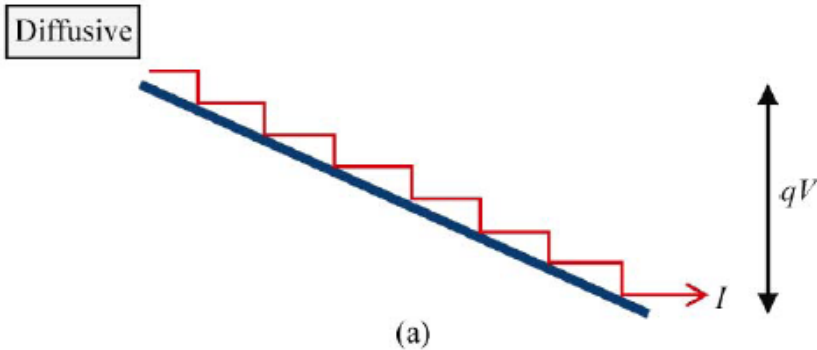


X. P. Wang et al. IEDM 2012



Yuan Heng Tseng et al., IEDM 2009

# Pre- or in-cell-resistor needed to scatter charge



Eric Pop, Nano Res (2010)

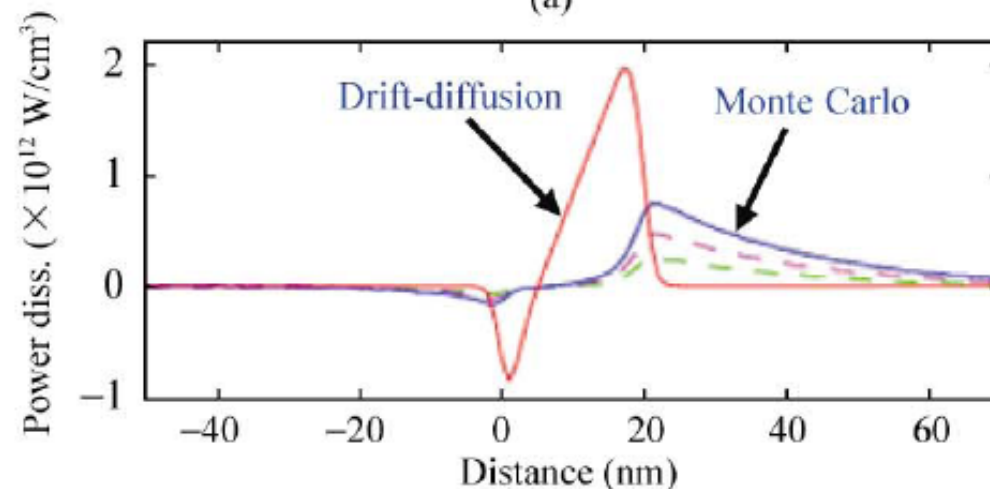
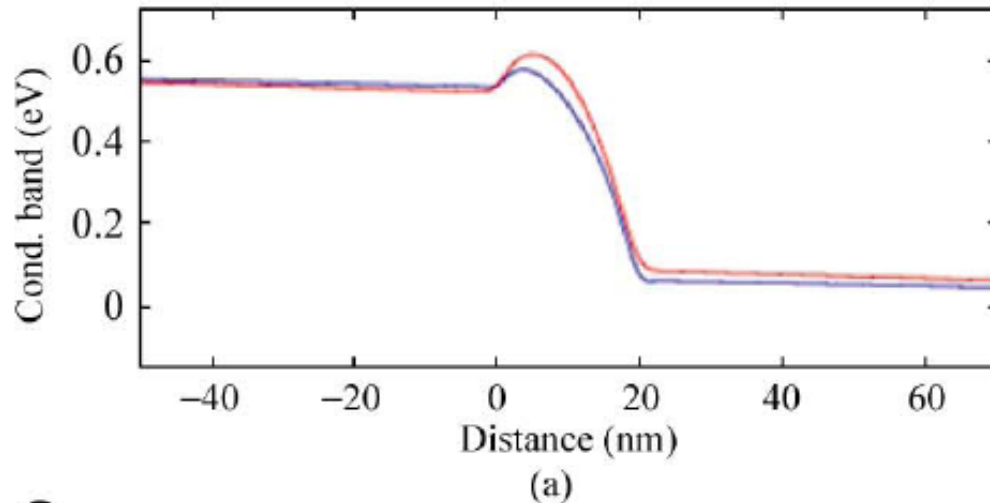
- ❑ Resistance comes from charge scattering
- ❑ cell-oxides are thinner than the mean free path:
  - ❑ therefore we have no scattering
  - ❑ on-resistance is fraction of  $R_{\text{Klitzing}}$
  - ❑ multiple quantum channels are formed
- ❑ best would be
  - ❑ High resistance path for the electrons
  - ❑ smooth forming – no cap discharge
- ❑ **Need built-in resistor!**

# At nano-scale classical continuum is not valid

$$P_V = jE$$

This classical equation is **not valid** on the scale of **mean free path**

electrons **relax deep** in the **contact**  
 → no **direct heating** in the MeOx channel  
 → **heat spreads** from **contact to filament**



Eric Pop, Nano Res (2010)

# How to operate at low currents

**in-cell resistor**  
 $d > \lambda_e$

**thicker oxide**  
**multiple layers**

**higher  $V_{form}$**

**need cap-**  
**layer for  $V^0$**   
**engineering**

**no retention**  
**strong T**  
**dependence**

**out-of-cell**  
**resistor**

**no-C resistor**

**use contact**  
**resistance**

**bad area**  
**scaling**

**huge serial**  
**resistance**

**capacitance**  
**reduction**

**only possible**  
**for academic**  
**samples**

**a densely**  
**packed array**  
**has high C**

**deal with a**  
**high C layout**

**use Active**  
**Feedback**  
**Cell**

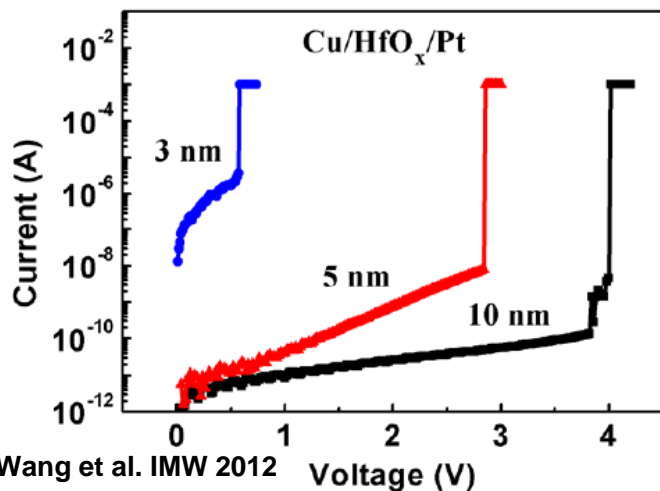
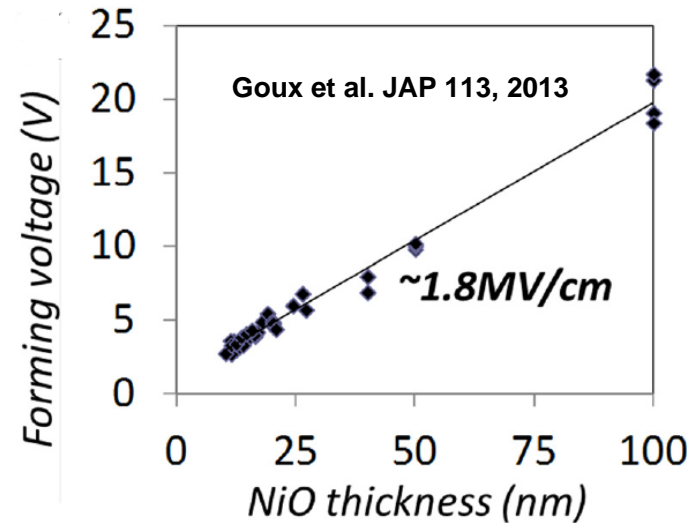
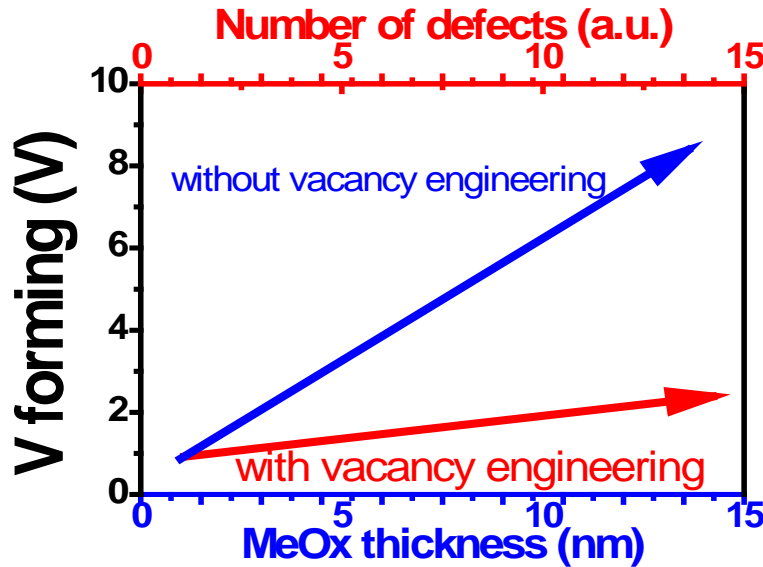
**with middle**  
**layer**

**with transistor**

**best: with**  
**vertical FET**

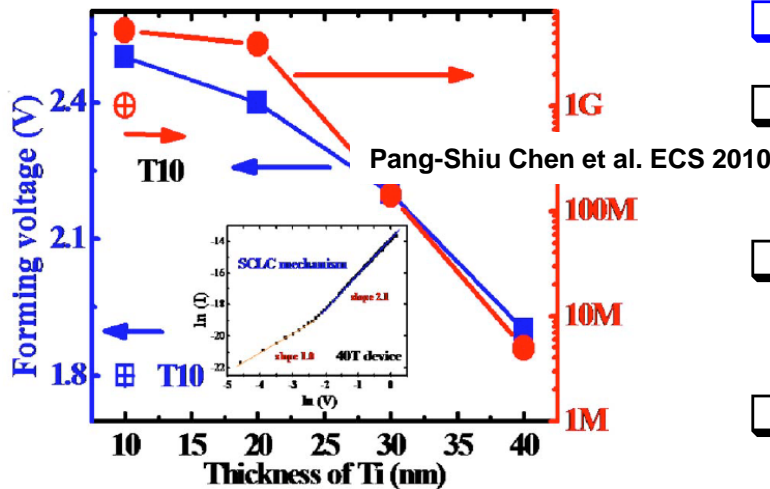
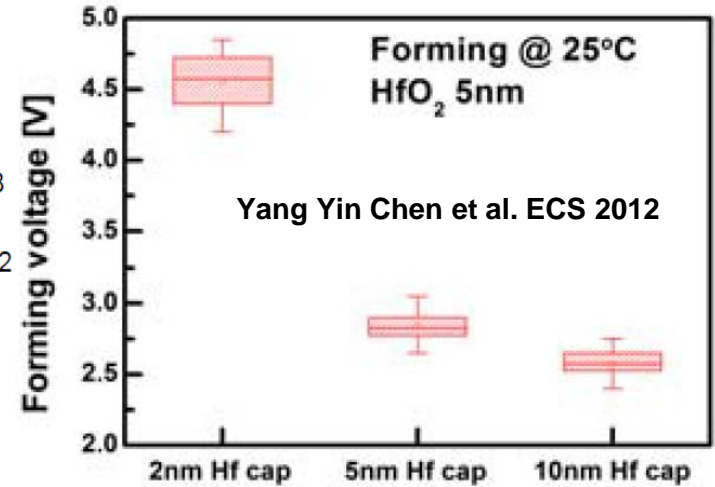
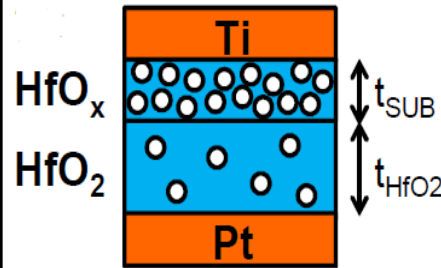
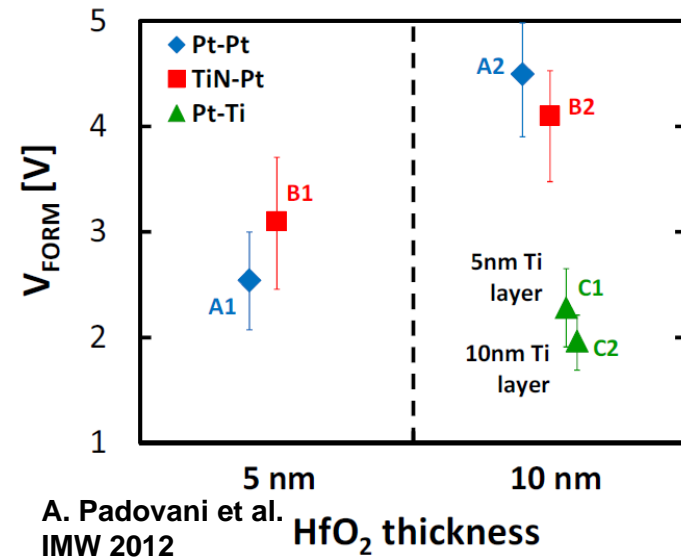
**diode does**  
**not work**

# In-cell resistor: MeOx thickness $d > \lambda_e$ (mean free path)



- Need to increase **thickness of MeOx** over **mean free path** to get scattering
- Forming voltage increases**
- Needs to be compensated by **vacancy engineering** (Getter material like Ti, Hf, Ta ...)

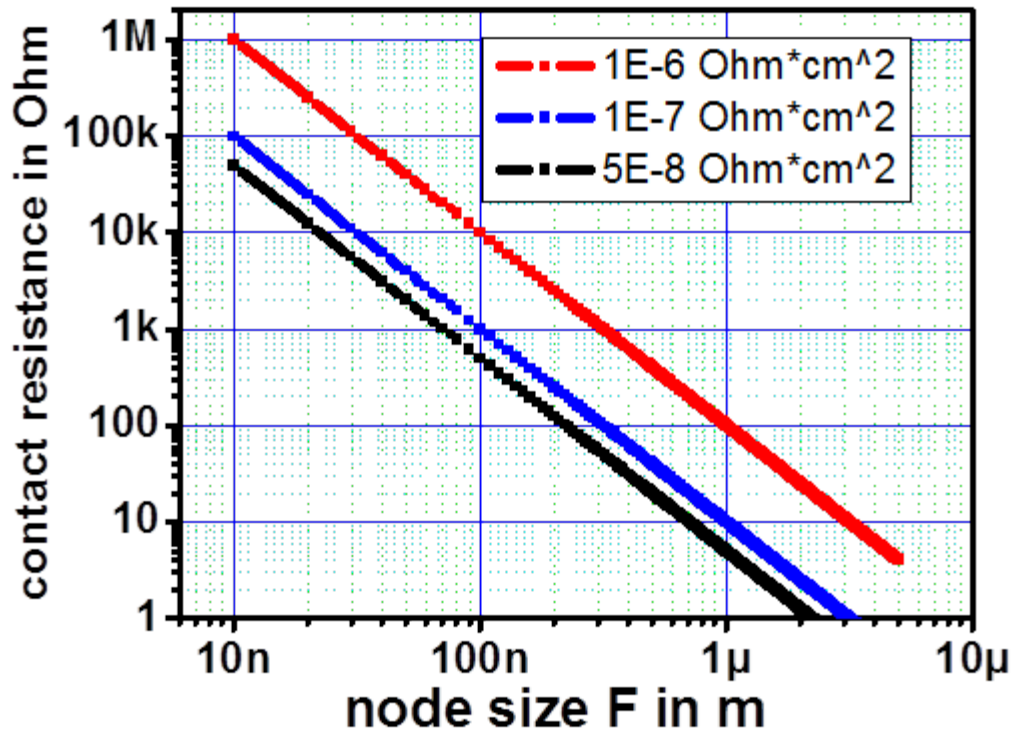
# Vacancy engineering for reduction of $V_{\text{forming}}$



- Works by depleting MeOx!
- Not in all case homogeneously (Ellingham diagram)
- Strong dependence on temperature budget
- Still has the problem of cap-discharge



# Current capping by contact resistance



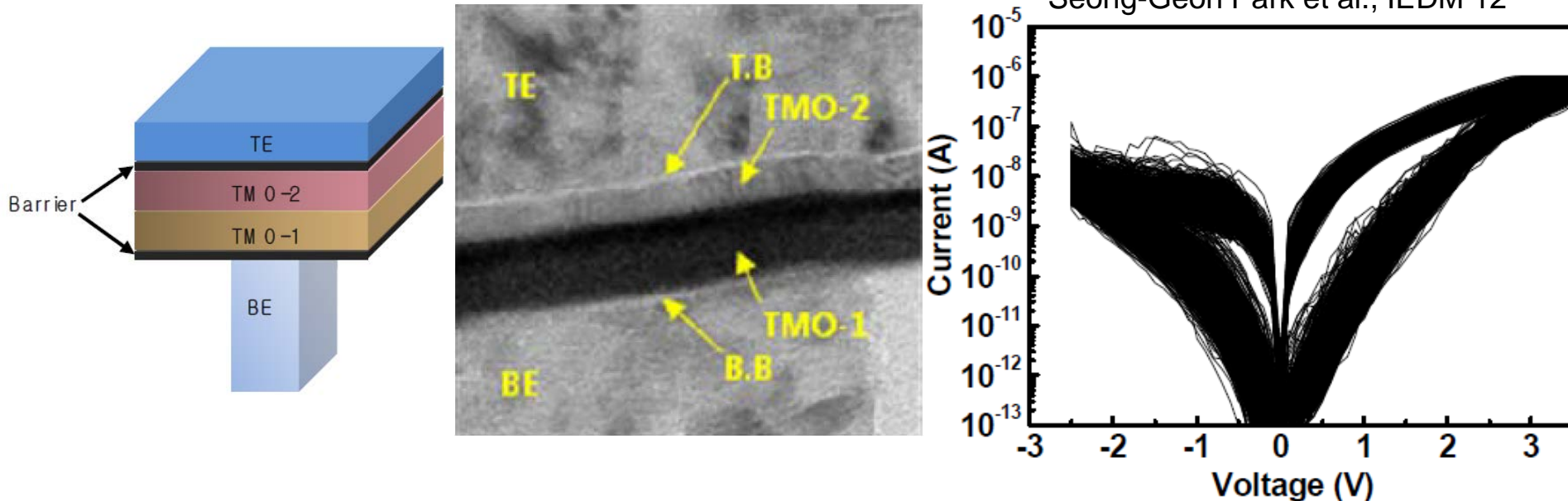
we have 2 contacts for a cell!

voltage drop at contact

J	\ CR	1E-6	1E-7	5E-8
10 MA/cm <sup>2</sup>		10 V	1 V	0.5 V
1 MA/cm <sup>2</sup>		1 V	0.1 V	0.05 V

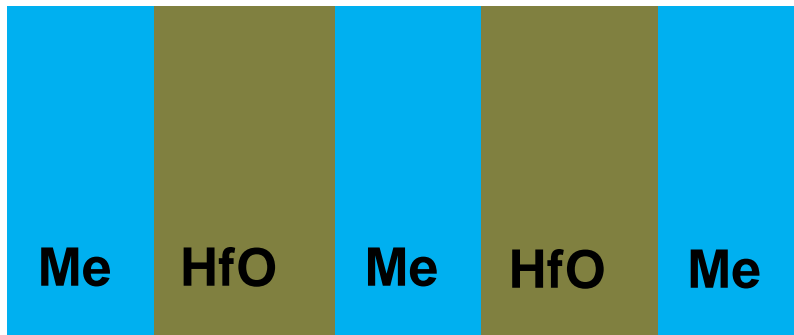
- ❑ Contact resistance (CR) contributes severely to overall resistance path
- ❑ Scales with area – what worked at ~100 nm, doesn't at ~10 nm!
- ❑ Associated voltage drop at high current densities is high

# Current capping by contact resistance



- ❑ From TEM one see thick MeOx ( $> 25$  nm) and contact resistance by additional barriers
- ❑ High voltage already at very wide cell (cell width not given in paper, but from TEM  $d > 100$  nm)
- ❑ Associated voltage drop at reduced cell size will be huge!

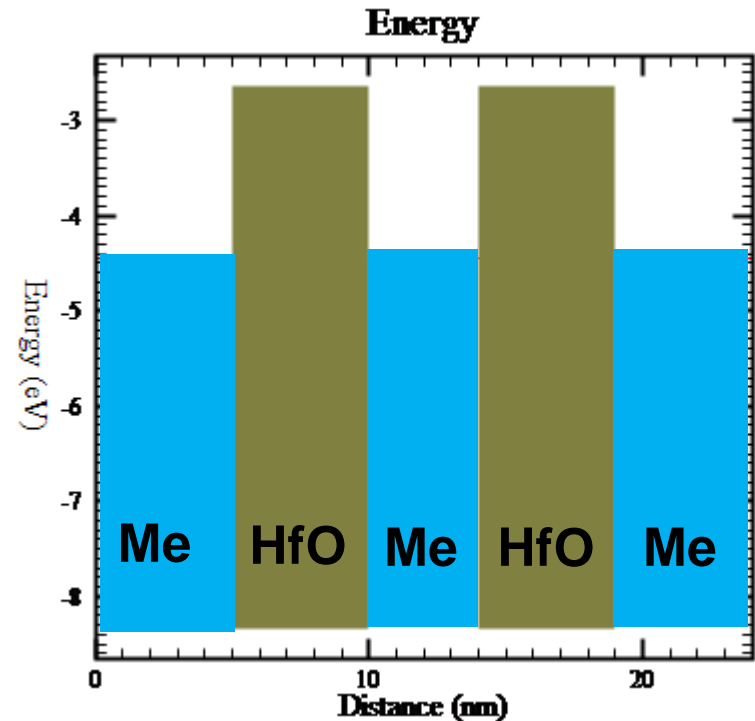
# Active Feedback Cell



**Me:** metal or highly doped Si

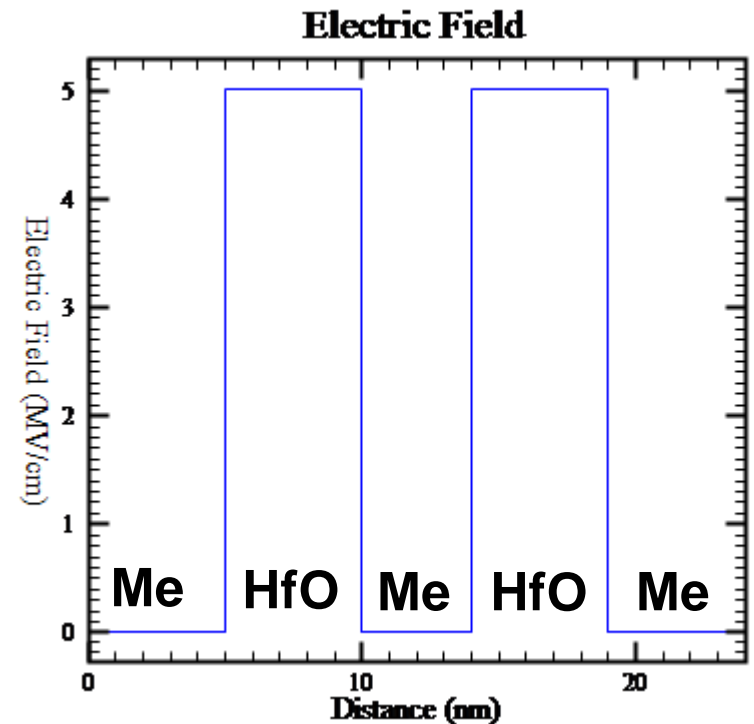
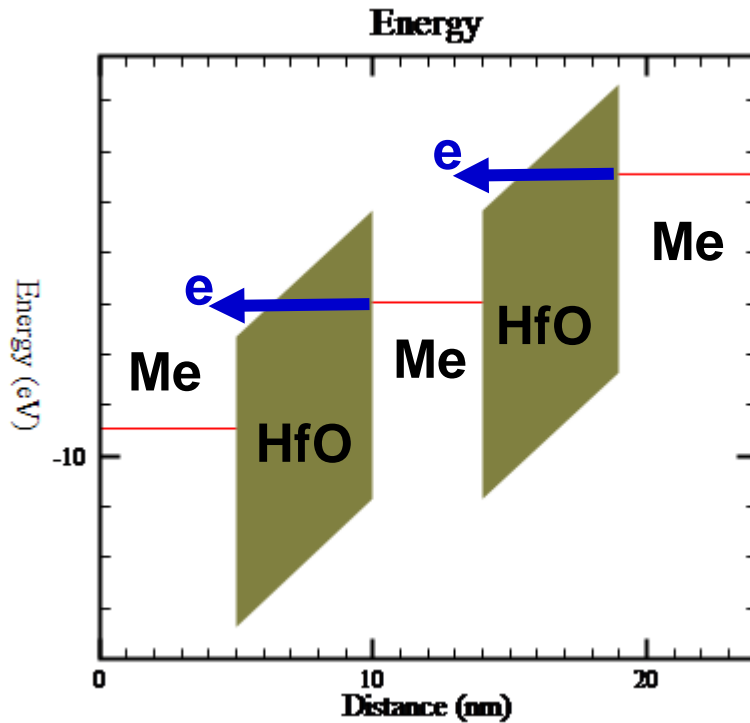
**HfO:** any switchable MeOx with capping layers for vacancy engineering

- Consider this double-barrier structure (this is not a CRS cell!!!)
- This has no forming overshoot due to built-in active feedback



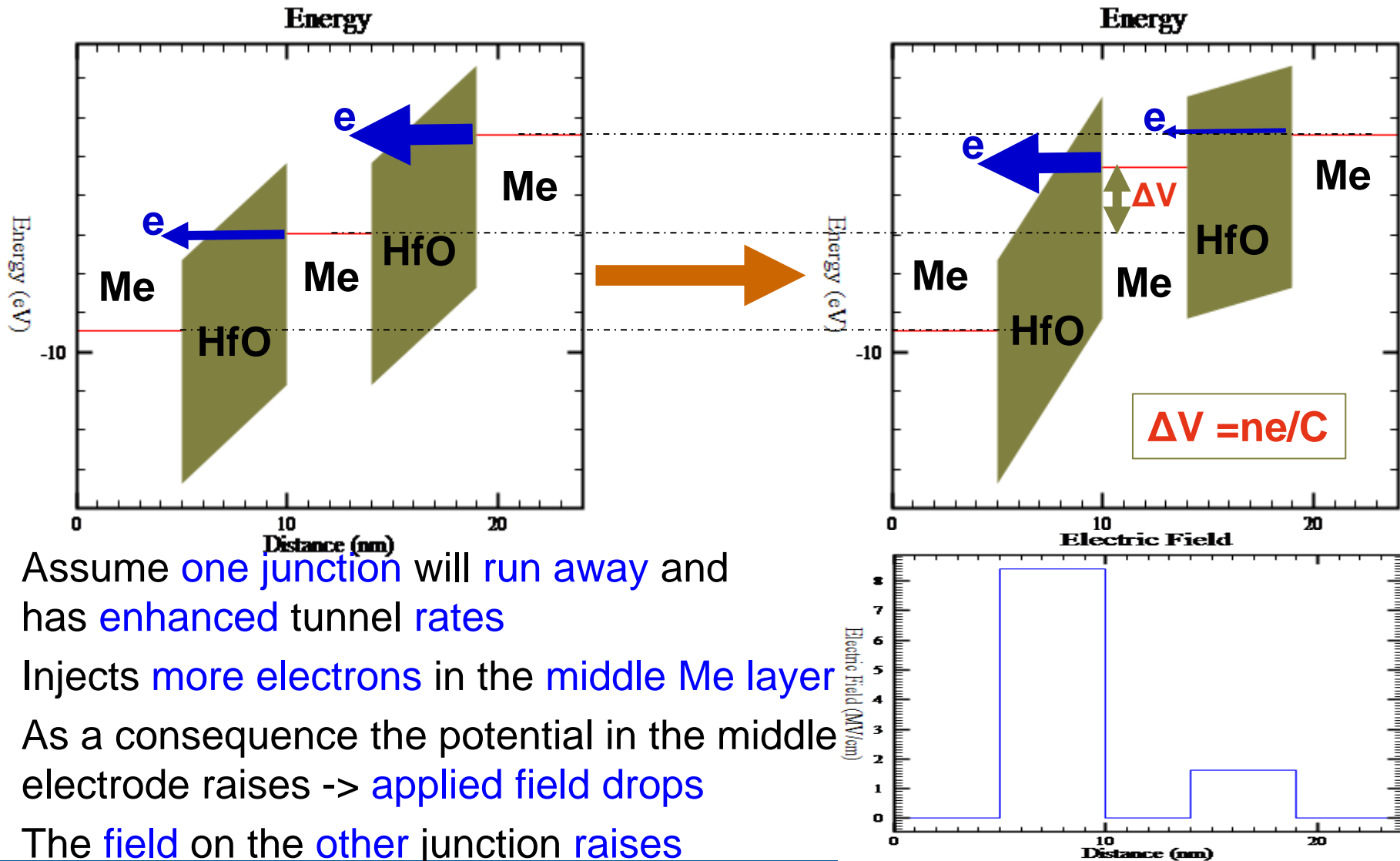
Kreupl et al., US 2011/0310654 A1  
 US 2011/0310655 A1  
 US 2011/0310653 A1

# Active Feedback Cell



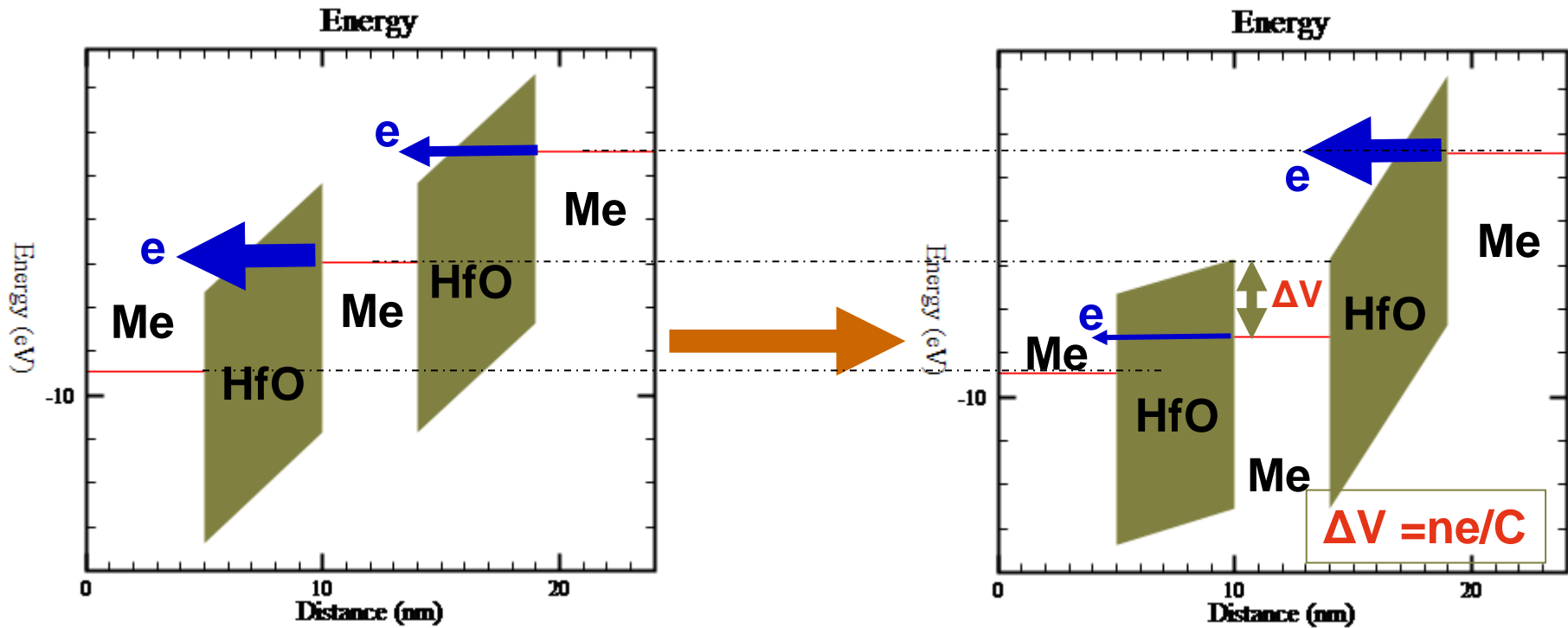
- ❑ For forming, a **voltage** is applied to the **outer Me electrodes**
- ❑ The **field drops** on the **HfO** layers and leads to **O-movement**
- ❑ The **electron tunneling rate** is almost **equal** for **both layers**, as I will show on the next slide and **limits overshoot** by **active feedback**

# Active Feedback Cell



- Assume **one junction** will **run away** and has **enhanced tunnel rates**
- Injects **more electrons** in the **middle Me layer**
- As a consequence the potential in the middle electrode raises -> **applied field drops**
- The **field on the other junction raises**

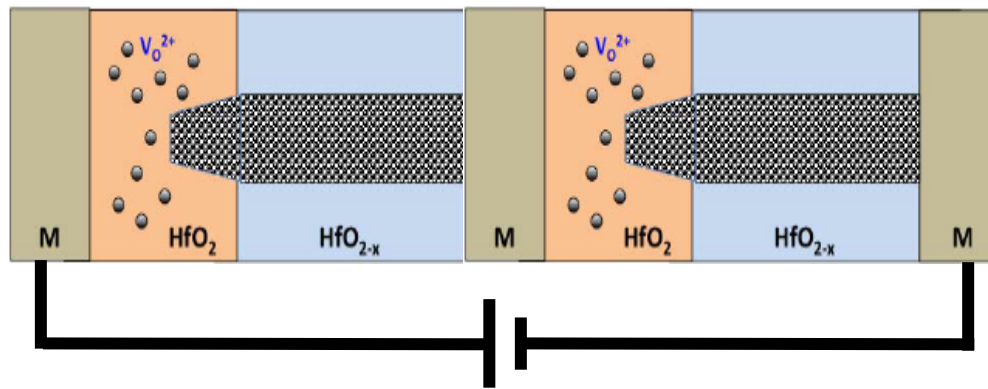
# Active Feedback Cell



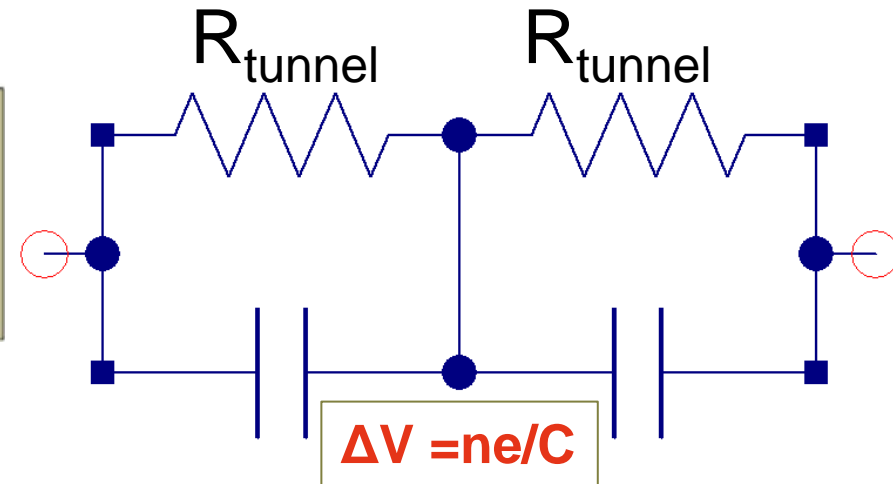
- Works **the same** if the **other junctions breaks** down
  - The capacitance of the middle electrode determines the active feedback voltage
- $$\Delta V = ne/C$$
- Works **instantly** and well with diode as selector



# Active Feedback Cell

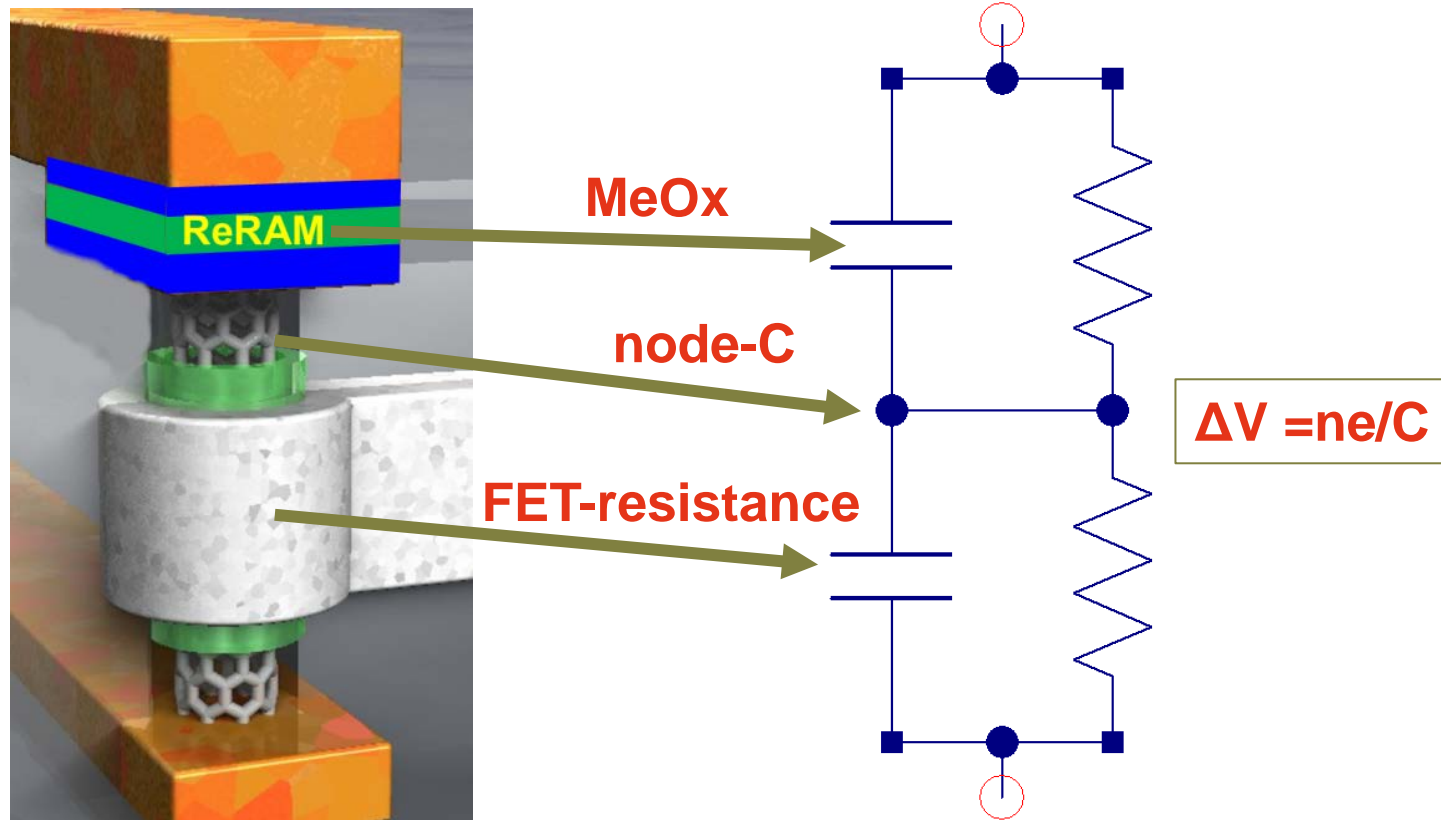


equivalent circuit



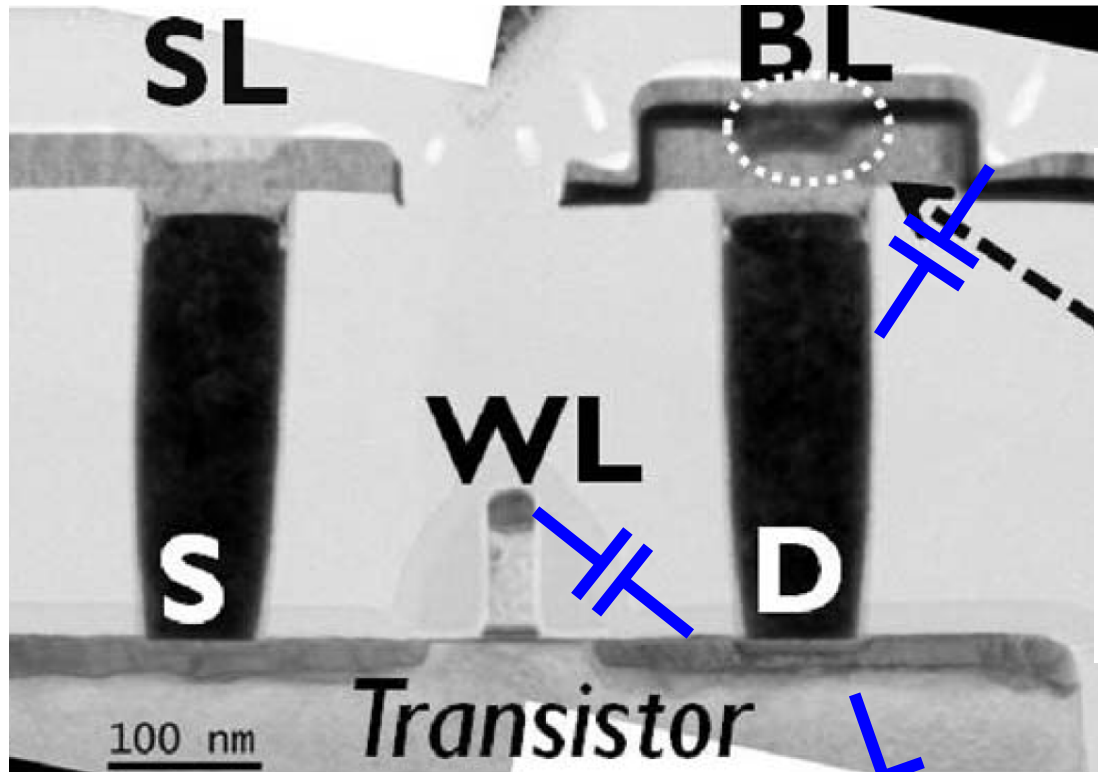
- ❑ Two filaments will form, but current overshoot is tamed by active feedback structure (like over-programming protection in floating gate NAND)
- ❑ The active feedback voltage depends on node capacitance of the middle electrode:
- ❑ for 1 fF:  $\Delta V = 1.6 \text{ V}$  for 10,000 electrons and current of  $dQ/dt = 1.6 \mu\text{A}$
- ❑ for 10 fF:  $\Delta V = 1.6 \text{ V}$  for 100,000 electrons and current of  $dQ/dt = 16 \mu\text{A}$

# Active Feedback Cell (single junction) with FET

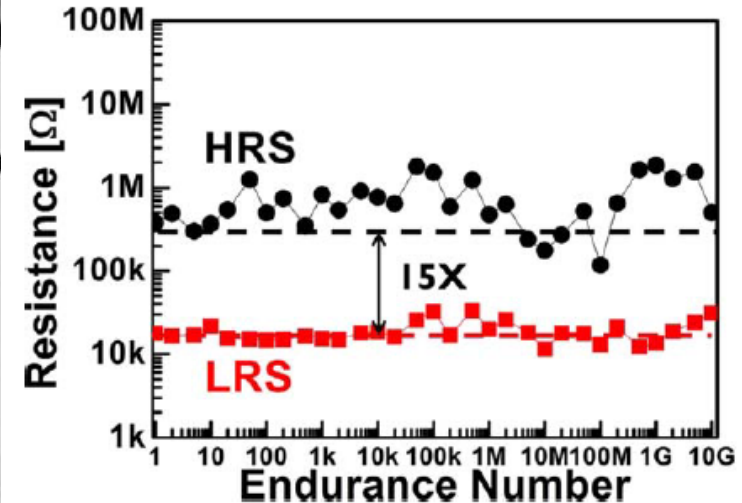


- ❑ Works also in **single junction mode**, if **input** capacitance of FET **is low** - small diffusion capacitance –best is vertical FET!!
- ❑ Does **not work** with **diode** – rf-model of diode is capacitor

# Planar FET might have too high capacitance



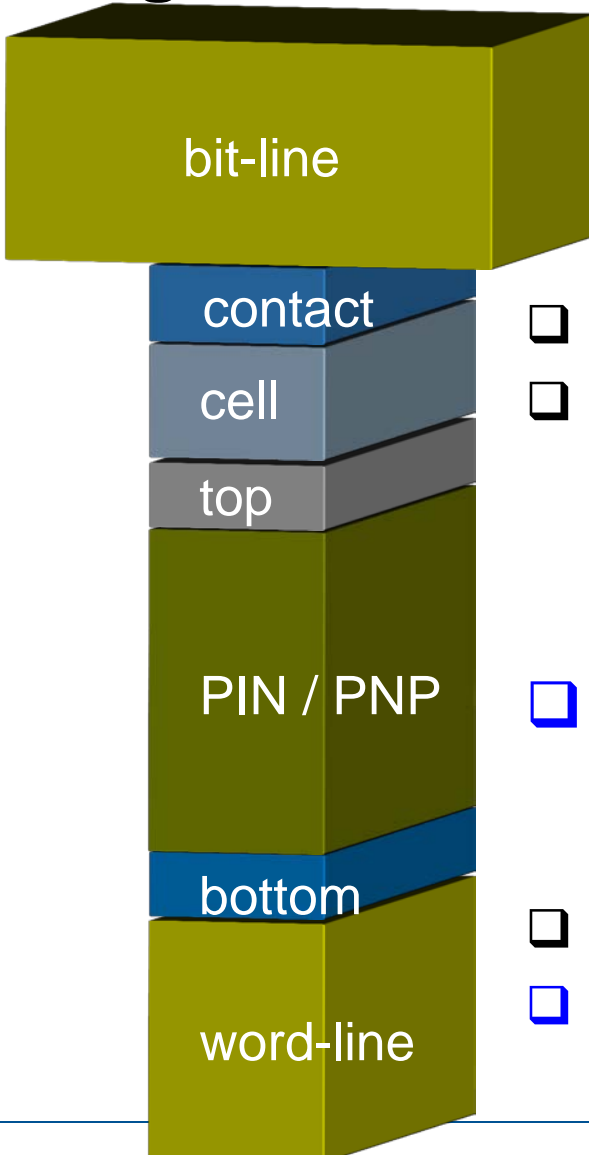
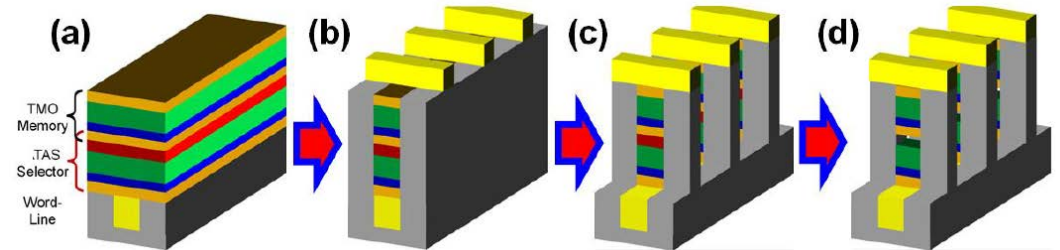
Yang Yin Chen et al., TED 2012



- ❑ Therefore only **low on-state resistance** cycling is possible
- ❑ But **10 G cycles** have been obtained by **short pulses**

# Integration challenges from SAPD

ChiaHua Ho et al., IEDM 12



- ❑ cost-effective integration requires SAPD
- ❑ etching of complicated high aspect structure:
  - ❑ sidewall implants in cell and diode from RIE
  - ❑ diffusion of etch species in carefully designed memory cell...
- ❑ etch-clean in complicated structures
  - ❑ How to clean etch damage in diode and memory cell?
- ❑ all "vacancy engineering" is gone after a plasma ash
- ❑ "all surface" effects dominate in sub 20 nm

## Summary

- ❑ There is **no memristor – cap-discharge** is the culprit
- ❑ **Oxygen vacancy ReRAM** looks most promising
- ❑ Key is
  - ❑ **reduction** in operating **currents** and
  - ❑ achieving **higher on-state** resistance
- ❑ **Current overshoot** creates several **quantum channels** in the ReRAM cell, which have low resistance
- ❑ Four methods have been proposed to **mitigate current overshoot**
- ❑ **Active Feedback Cell** with vacancy engineering is most promising
- ❑ Key challenge: **how stable** are **low current states**?  
**most MeOx** studied at **high j** - what will be the **right material**?