

Department of Hybrid Electronic Systems

Carbon Memory Assessment

A white paper for the ITRS ERD meeting on August 25-26, 2014, Albuquerque, NM can be downloaded here: http://arxiv.org/abs/1408.4600

Franz Kreupl

Technische Universität München (TUM) Department of Hybrid Electronic Systems (HES) franz.kreupl@tum.de



Outline: Carbon Memory Assessment

Basic Facts about Carbon

- Carbon Allotropes
- Manipulating the Bond Structure of Carbon
- Sustainable Current Density in Carbon Structures
- Break-junctions and Plumbing in Carbon Structures
- What Is Not Considered as Carbon-based Memory
- Carbon-based Resistive Memory Phase Diagram
- First Current Pulse Challenge with Conductive Carbon
- Forming Challenge in Insulating Carbon
- Scaling of Carbon Memory
- Architectural Challenges for Resistive (Carbon) Memories
- Current State-Of-The Art For Carbon Memory Technology
- Selected Literature



Basic Facts about Carbon

 Carbon materials can have very different mass densities: 4 mgcm-3 for nanotube-based aerogels
 0.2 - 1 gcm-3 for porous carbon
 2.2 gcm-3 for graphite
 3.5 gcm-3 for diamond

- The electronic properties range from metallic to semiconducting to insulating,
- The mechanical behavior cover everything, from soft to very hard

Graphite is the most stable form and all other forms, especially sp3-based bonds in diamond and ta-C favor the relaxed sp2-bond



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The Well-known Carbon Allotropes



Graphene

Single-walled CNT

Multi-walled CNT



The Lesser-known Carbon Allotropes: a-C:H



Yellow balls represent one-fold carbon atoms, red balls are two-fold (sp1) atoms, white balls are three-fold (sp2) atoms, cyan ones are four-fold (sp3) atoms, and blue ones are hydrogen atoms



<u>The Lesser-known Carbon Allotropes: a-C:H</u>





The Lesser-known Carbon Allotropes: ta-C





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I tetrahedral amorphous carbon (ta-C) is produced by filtered cathodic vacuum arc (FCVA), mass-selected ion beam (MSIB), magnetron sputtering or laser ablation: temperature stable up to 900 C



The Lesser-known Carbon Allotropes: ta-C



ta-C with high density with high stress
 stress can induce a transformation from sp2 – to sp3



The Lesser-known Carbon Allotropes: low mass density porous carbon, foam, ribbons....





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I can be formed from carbides (TiC, SiC), pyrolysis of hydrocarbons, or spin-on deposition of carbon nanoparticles, fullerens or nanotube solution,



Manipulating the Bond Structure of Carbon

- By stress relaxation, e-beams, electrical current, laser pulses, x-rays or temperature.
- Graphitization usually happens at above 2500 K,
- Small current can heal defects in nanotubes and graphene and even lead to the transformation of amorphous carbon into sp2-type carbon
- The power per volume is given by j²·ρ, (current density j and the specific resistivity ρ)
- 100 nA focused on a filament with 1 nm² cross-section, gives 10 MA/cm² !!
- Delivered power density is MW/cm³ to GW/cm³



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Manipulating Bonds by Laser Pulse



- Short laser pulse induces disorder (D-band)
- D-band overlaps with sp³-peak at 1332 cm⁻¹
- Diamond cubic phase observed by e-beam diffraction
- Disordered, quenched state by short energy pulse

Bonelli et al., Laser-irradiation-induced structural changes on graphite, Phys. Rev. B 59, 13513 (1999)

 $0 2\overline{2}$

 $1 \, 1 \overline{1}$



Manipulating Bonds by Laser Pulse

- An increase of the average crystalline size of graphitic clusters occurs upon radiation performed at fluences of 300 and 400 mJ/cm²,
- At higher energy density the material undergoes complete amorphization.
- Graphitization or, conversely amorphization of glassy carbon surface layers can be achieved by a proper choice of the laser irradiation conditions.

Carbon behaves like a phase change material

G. Vitali, M. Rossi, M. L. Terranova, and V. Sessa, Laserinduced structural modifications of glassy carbon surfaces, J. Appl. Phys. 77, 4307 (1995)



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Manipulating Bonds by Current Increase of current



By driving current thru the amorphous carbon (with high resistance), carbon is transformed into aligned sp2bonded structures with low resistance

A short current pulse can transform the crystallized carbon again into an amorphous structure



Manipulating Bonds by Current: CNT Bucky Paper



Jin Gyu Park, Shu Li, Richard Liang, Chuck Zhang, Ben Wang, Structural changes and Raman analysis of single-walled carbon nanotube buckypaper after high current density induced burning, Carbon 46, 1175 – 1183, (2008)

"In the broken area, nanotubes existed only on the surface and TEM & Raman show that the CNT structures were completely changed into other structures such as a graphite sheet or nanohorn, or a large diameter SWCNT other graphitic structures"



Sustainable Current Density in Carbon Structures

- Sustainable current density is as high as 400 MA/cm² in graphitic carbon or even up to 1GA/cm² in SWCNT
- In porous carbon structures, the observed sustainable current densities are much lower and depend on the mass density of the carbon material.
- In porous carbon structures the current carrying parts have also high current densities, but averaging over the whole volume makes it drop
- Current pulse duration in carbon needs to be as short as possible because otherwise surrounding material is destroyed and metallic electrodes molten.



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Sustainable Current Density in MWCNT





MWCNT on SiN membran

Prior to complete failure SiN dissociates at ~ 2173 K
 hot carbon destroys other materials
 CNT fails at ~200 MA/cm2 at ~3200 K
 Current pulses needs to be as short as possible

1000 500

T. D. Yuzvinsky, W. Mickelson, S. Aloni, S. L. Konsek, A. M. Fennimore, G. E. Begtrup, A. Kis, B. C. Regan, and A. Zettl, Imaging the life story of nanotube devices, APL 87, 083103, (2005)



Sustainable Current Density in MWCNT





Sustainable Current Density in Graphenic C





❑ Critical current density of 350 MA/cm² observed
 ❑ Appropriate cell diameter ~ 6 nm for I < 100 µA
 → Use spacer, cladding or self-assembled nano-pores

F. Kreupl, et al., Carbon-Based Resistive Memory, Proceedings of the IEDM, 521, (2008)



Sustainable Current Density in Electrodes



R. Zou , Z. Zhang , Q. Liu , K. Xu , A. Lu , J. Hu , Q. Li ,Y Bando , D Golberg, Melting of Metallic Electrodes and Their Flowing Through a Carbon Nanotube Channel within a Device. Adv Mater., 25(19),2693-9, (2013)

□ A CNT in contact with a Au electrode
 □ At 1.5 V and 27µA the Au electrode melts and fills the CNT
 → high current density not suitable for metallic electrodes
 → keep current pulses as short as possible



Break-junctions and Plumbing in Carbon Structures

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- Break junctions can be created in carbon structures operated in open systems (like in a TEM, vacuum probe station, even in air) if the critial current density is reached.
- On/Off switching is observed in break junctions once a critical electric fields is achieved.
- This can be explained by trapping of hydrocarbon gas between the junction and subsequent pyrolysis in a bad vacuum (10⁻⁷ mbar equals ~ 3.10⁹ molecules/cm³).
- Break junctions can also be created in porous carbon that is encapsulated.
- Carbon structures separated by a short gap can be plumbed together by the application of an electric field. Joule heating from the field emission current will cause atom diffusion and rearrangement of carbon. Typical currents: 0.5 μA - 10 μA



Break-junctions and Plumbing in Graphenic C



B. Standley, W. Bao, H. Zhang, J. Bruck, C. N. Lau, M. Bockrath, Graphene-Based Atomic-Scale Switches, Nano Lett., Vol. 8, 13, 3345-3349, (2008)





Alexander Sinitskii, James M. Tour, Lithographic Graphitic Memories, ACS Nano Vol.3, No. 9, 2760–2766, (2009)



Hydrocarbon Contamination in 10-7 mbar Vacuum



Figure 5. X and Y enlargement of the corner region due to contamination and drift in a CD-SEM. 800 V, 3 pA electron beam bombardment for 6 minutes.

Even in vacuum of 10⁻⁷ mbar, 3-10⁹ molecules/cm³ are present
 E-beam in SEM deposits this as carbon contamination on the sample

□ The hydrocarbons can also be trapped by an electric field

Vladar, A. E., Postek Jr, M. T., & Vane, R. (2001, August). Active monitoring and control of electron-beam-induced contamination. In 26th Annual International Symposium on Microlithography (pp. 835-843). International Society for Optics and Photonics.



Break-junctions and Plumbing in Graphenic C



Trapping of hydrocarbons debris in a CNT-switch upon the application of an electric field
 Likely to be the main reason for on/off switching in open systems (TEM, vacuum probe station)

Peter Ryan, Yu-ChiaoWu, Sivasubramanian Somu, George Adams, Nicol McGruer, Single-walled carbon nanotube electromechanical switching behavior with shoulder slip, J. Micromech. Microeng. 21, 045028, (2011)



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Break-junctions and Plumbing in SW-CNTs



on-state off-state switch on on-state 12 uA 6 uA, 1.6V

Chuanhong Jin, Kazu Suenaga, Sumio Iijima, Plumbing carbon nanotubes, Nature Nanotechnology 3, 17 - 21, (2008)



Break-junctions and Plumbing in CNTs



When 1.0 V is applied between the MWNTs, the current increases to 15.6 µA and tips A and B coalesce at portions of the outermost wall layers

Koji Asaka, Motoyuki Karita, Yahachi Saito, Joining of multiwall carbon nanotubes for the endcontact configuration by applying electric current, Materials Letters 65,1832–1834, (2011)



Break-junctions and Plumbing in CNTs



Atsuko Nagataki, Takazumi Kawai, Yoshiyuki Miyamoto, Osamu Suekane, Yoshikazu Nakayama, Controlling Atomic Joints between Carbon Nanotubes by Electric Current, PRL 102, 176808, 26 (2009)



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Break-junctions and Plumbing in Graphene





" Under such high activation energy due to high current heating, the attaching edges of two opposite GSs undergo atoms' activation, diffusion and reconstructing to rearrange the carbon networks, such as hexagonal rings, pentagon-heptagon pairs, for seamless joining"

Rujia Zou, Zhenyu Zhang, Kaibing Xu, Lin Jiang, Qiwei Tian, Yangang Sun, Zhigang Chen, Junqing Hu, A method for joining individual graphene sheets, Carbon 50, 4965–4972, (2012)



What Is Not Considered as Carbon-based Memory

- diffusing metal ions into insulating phases of carbon to form a resistive memory effect based on metal filament creation and annihilation [36, 37, 38, 49]
- metal diffusion occurs in almost all situations (like in ref. [37, 49]) where the capacitance discharge current from the first forming event is done by dc-voltage sweeps on samples with no on-chip current limiter, like on-chip resistors or transistors
- SMU can neither limit the capacitance discharge current nor a dc-current on a time scale shorter than ~30 µs
- also not considered: electronic memory effects in insulating forms of carbon films. The injected charge carriers modulate the tunnel barriers, but this is a volatile effect.



Carbon-based Resistive Memory Phase Diagram



two different mechanism

- Iow mass density: break-junction by local evaporation of carbon and plumbing by field emission
- □ high mass density: conversion of $a-C \leftrightarrow sp^2$ -bonds



Break-junctions and Plumbing in Porous Carbon



low conductance

high conductance

- Field emission currents lead to rearrangement of the C-atoms and finally bridge the gap
- sp²-bonds bridge a nano-gap in porous carbon (on-state).
- The sp²-bridge is deconstructed by a current pulse (~10 μA)
- Inherently scalable to atomic bonds



Amorphous Carbon to sp²-Bonds Conversion sp³ sp²



sp² to sp³ conversion of disordered graphitic carbon (phase change of carbon)

inherently scalable to atomic bonds (no phases of different materials) 31



First Current Pulse Challenge with Conductive Carbon



- □ First (!) current pulse needs to destroy all conducting paths
- The required current density (400 MA/cm²) is too high for high mass density graphenic carbon
- Porous carbon might be accessible with ~10 MA/cm²



Forming Challenge with Insulating Carbon



- Capacitance discharge currents (C*dV/dt) define R_{on}
- On-chip current limiter are needed (transistors)
- Forming voltage should be as low as possible (tunable by C-thickness)



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Typical Cap-discharge Current (C*dV/dt)



 Typical pad and probe tip have C > 1 pF
 Speed is within rise time of the scopes
 Relevant capacitance is within a sphere of r = t*v_{prop.} <100ps*v_{prop.} (Wahlgren – horizon picture)

My experience: cell R_{ON} is defined by first (forming) C*dV/dt
 That's the reason why most ReRAM data have the same low
 R_{ON}, (<~ 20 kOhm) independent of the used material or stack
 I_{cap} reduction techniques include on-chip current limiter and high temperature forming



Scaling of Carbon Memory

Scaling of carbon memory can go down to individual atomic bonds
 Open question are how much voltage and current is needed to create, maintain or destroy the atomic bonds
 Reported currents are around and below 10 µA



La Torre, A., Romdhane, F. B., Baaziz, W., Janowska, I., Pham-Huu, C., Begin-Colin, S., ... & Banhart, F. (2014). Formation and characterization of carbon–metal nano-contacts. *Carbon*, 77, 906-911.



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Scaling of Carbon Memory: structural examples



Casillas, G., Mayoral, A., Liu, M., Ponce, A., Artyukhov, V. I., Yakobson, B. I., & Jose-Yacaman, M. (2014). New insights into the properties and interactions of carbon chains as revealed by HRTEM and DFT analysis. *Carbon, 66*, 436-441.

Individual carbon chains show high resilience, but long time stability it is currently not known



Scaling of Carbon Memory: porous carbon very high variability is expected once the structure size scales down to the size of the constituents (CNTs, voids ect.) example CNT ribbon:



 □ depending on the location of the top electrode (blue), there will be a void or a lot of CNTs → high variability
 □ more accurate assembly is required (aligned SWCNTs) to make variability smaller



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Scaling of Carbon Memory: Contact Resistance



voltage drop at one contact:				
J \ CR	1E-6	1E-7	5E-8	
10 MA/cm ²	10 V	1 V	0.5 V	
1 MA/cm ²	1 V	0.1 V	0.05 V	

 Biggest threat for scaling (ReRAM) might come from contact resistance
 Scales with area – what worked at ~100 nm, doesn't at ~10 nm!
 Associated voltage drop at high current densities is very high



Architectural Challenges for Resistive Memories



□ In advanced nodes the interconnect wiring plays an active element due to IR-drop and RC-delay in wires & contacts

Operating with fast pulses will be challenging or impossible
 A possible solution would be to operate the memory array in the capacitance discharge mode:

The interconnect wires are precharged to V by the x-access point while the y-access is still floating. After precharging, the x-access is is disconnected. The energy $\frac{1}{2}$ CV² that is stored in the interconnects is discharged to ground or even negative voltage by enabling the y-access.

This approach guarantees that the wiring is discharged after the pulse and no set after reset can happen



Fu, D., Xie, D., Feng, T., Zhang, C., Niu, J., Qian, H., & Liu, L. (2011). Unipolar resistive switching properties of diamondlike carbon-based RRAM devices. Electron Device Letters, IEEE, 32(6), 803-805







Fig. 4. Reliability tests of the DLC-based RRAM devices. (a) Switching for 1000 cycles. (b) Data retention at 300 °C for 600 min under Ar atmosphere.

Only single cells This work has high capacitance layout Real time-resolved switching currents are not measured, but for set, at least an external current limiting resistor has been used Good data retention at 300° C for 600 min



Current State-Of-The Art For Carbon Memory Technology

Dellmann, L., Sebastian, A., Jonnalagadda, P., Santini, C. A., Koelmans, W. W., Rossel, C., & Eleftheriou, E. (2013, September). Nonvolatile resistive memory devices based on hydrogenated amorphous carbon. In Solid-State Device Research Conference (ESSDERC), 2013 Proceedings of the European (pp. 268-271). IEEE.



Only single cells, 18 nm thick a-C:H film

High capacitance layout

Demonstrates what is needed: time-resolved current to be measured starting from the first forming event to reset & set
 On-chip resistor has been used to limit current overshoot



Current State-Of-The Art For Carbon Memory Technology The most advanced studies with results from 4 Mb arrays are based on porous CNTribbon memory from the company Nantero (References [44, 45, 46, 47, 48])



Rosendale, Glen, et al. "A 4 Megabit Carbon Nanotube-based nonvolatile memory (NRAM)." *ESSCIRC, 2010 Proceedings of the*. IEEE, 2010.



4Mb arrays in 0.25 µm CMOS, some 20 nm cells are reported
 First pulse requirements are not reported and might be high
 10¹¹ endurance cycles on some cells with high capacitance layout are reported with 20 ns pulses (VLSI 2014)
 Switching currents vary and are estimated from gate voltage on huge transistor biased close to V_{th} (which have big variations) or are measured on individual cells to be in the order of 20-30 µA
 Overall, the published data are somewhat inconsistent (SEM shows 250 nm cell, text says 140 nm etc..)



Challenge of Predicting Technology Performance

 Real Chip layout and technology are needed
 But these are proprietary data, which are not disclosed
 Example: well-known DRAM chips run same task, same JEDEC specs, different vendors and technologies



Even idle currents are 3x different!



		Unobtainable-		
		RAM	CARBON MEMORY	Comments
	Description	(e.g., "Ideally")		(including any associated tradeoffs)
	Scalability	Each layer @ 4F ² down to beyond 12nm node	@ 4F ² down to single atomic bonds	both memory cell AND wire pitch can be scaled. But care needs to be taken about the select device. Major threat comes from contact resistances
cost	Multi-level cells (MLC)	Up to 3bits/cell	2 bits/cell are demonstrated [48], Recommended is 1bits/cell	MLC in RRAM is possible for relaxed feature sizes. IF RC from interconnects play an important role only, Ron > 200 kOhm might be accessible
, size,	Multi-layer stacking	At least 32 layers	8-12 Multilayer might be possible	BEOL compatibility depends on the select device. Complicated stacks needs to be etched at 8-12 layer. 3D monolithic integration might be feasible
Scalability	Fabrication costs	Total cost very similar to current NAND or lower	Similar to PCM or RRAM	Number of critical mask steps= 1 for 1layer CMOS - No new/difficult unit processes -New/difficult materials only with nanotubes, a-C is known to be compatible with CMOS processing- device forming is necessary (first pulse challenge)!
	Array efficiency	>100% (circuitry tucked underneath, w/ extra Si real-estate left over)	Similar to PCM or RRAM	 BL/WL lengths Extent of peripheral circuitry Peripheral circuitry play a critical role (such as compliance, or current limiting needed for low power Interplay with 3D stacking



		Unobtainable-		
		RAM	CARBON MEMORY	Comments
	Description	(e.g., "Ideally")		(including any associated tradeoffs)
-əc	Array size	N/A (Unobtaina-RAM has not been demonstrated)	4 Mbit [45]	obtained individually
f-t	Yield	N/A	Not known	
State-of art	Technology node	N/A	20 nm cells demonstrated (in public domain) [45]	But not for both the implemented CMOS device AND for the wiring pitch (CMOS 0.25 μm) First current pulse issue not investigated
e ncy I-level and el. if known)	Read latency	< 10ns (for memory applications) (~1us for storage applications)	~50 ns for 1 [45] ~30 ns for 0 [45]	 read contrast ~1000 Size of read window Read disturb issues Errors from crosstalk all depend on chip design
Lato (Both cell svstem-levo	Write latency	< 20ns (for memory applications) ~1us for storage applications)	~20 ns [48]	 Requires verify-after-write/erase Write disturb of other devices = research Damage threshold to avoid? = research write-in-place supported all depend on chip design



		Unobtainable-		
		RAM	CARBON MEMORY	Comments
	Description	(e.g., "Ideally")		(including any associated tradeoffs)
/ Energy	Read power / Energy	< 1/10 scaled DRAM for memory applications (for storage applications, same as scaled NAND or better)	1V/10 nA 1V/10μA	 Power → parallelism → bandwidth Roadmap with scaling Please specify power usage by selected devices elsewhere in the array (leakage, line resistances), and in peripheral circuitry = depends on proprietary chip design
Powe	Write power / Energy	for memory applications, < 1/5 scaled DRAM (for storage applications, <5x read power)	15pJ/bit [48]	 Power → parallelism → bandwidth Roadmap with scaling? power usage by selected devices elsewhere in the array (leakage, line resistances), and in peripheral circuitry = depends on proprietary chip design



		Unobtainable-		
		RAM	CARBON MEMORY	Comments
	Description	(e.g., "Ideally")		(including any associated tradeoffs)
Reliability	Endurance	>>1e12 (memory applications) (>1e9, storage applications)	>1e11 [48]	 Can device failures be predicted research subject, scales with node Devices fail to what state? research subject, scales with node Do failed devices affect neighbors? research subject, depends on design Impact on other characteristics? (e.g., do cycled devices behave differently?) =research subject, scales with node Are failures random or clustered? = research subject, scales with node
	Retention	>1 month @ 85°C (memory) >10 years @ 150°C (storage)	>10 years @ 120°C 300 min @ 300 C [41] 168 h @ 250 C [44]	tradeoffs, between retention & write-speed, or retention & cycling? = research subject, scales with node
	Variability	Extremely low (e.g., 6 th -sigma device also meets all specs)	If we would have 6 sigma, we would have a product	Intra-device & inter-device – variability & repeatability? = research subject, scales with node Porous carbon will have a problem at small dimension



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