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Integration Challenges for Carbon Nanotubes

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1. Introduction

During the last years carbon nanotubes (CNTs) have become more and more important as a possible future electronic material. The possible applications range between field-emission structures in flat-panel displays to inter-connects, transistors, opto-electronics and even power transistor application [1]. The overall activity in this field is still increasing as the number of publications concerning CNTs shows. The publications are likely to peak in 2005 with over 4000 publications, as can be seen in Fig. 1. But whereas the basic investigations of nanotubes are ongoing, the application specific needs of integrating these objects are still in its infancy. In this presentation we discuss the status and challenges for CNT integration as interconnects, transistors and power transistors.

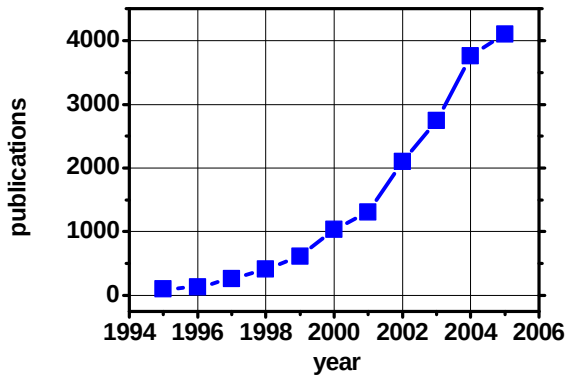

Fig. 1 The number of publications (including patent applications) for CNTs. The value of 2005 is extrapolated from early 2005 data.

2. Interconnects

The most feasible and early implementation of CNTs in microelectronic application could be their use as vertical interconnects in the metallization scheme [2,5]. Recent advances have demonstrated this approach to be scalable at least down to the 20 nm diameter via [3]. In Fig. 2 a 20 nm wide via is shown, which has been filled with a multi-walled CNT protruding out of the 150 nm deep via. Current densities exceeding 10^8 A/cm^2 have been measured for such CNT vias. The key questions to be solved for CNT vias are related to the filling factor, the quality of the CNTs and the contacts to the tubes. All this has to be achieved at a very low temperature budget of around 400-500 °C - to be compatible with backend of the line temperatures. The main challenge is to obtain catalyst particles at the bottom of the vias which after all processing steps are still capable to produce CNTs in a subsequent CVD-process. The most versatile approach is a buried catalyst approach [3], where the catalyst stack resides on top of the copper metal layer serves also as etch-stop during the via etch. Lift-off approaches are only suitable for low aspect ratio vias and do not support use of preformed clusters. The catalyst free growth of nanotubes is restricted to higher temperatures.
In contrast to these vertical interconnects, lateral CNT wiring in one metal layer are not yet feasible, although theoretical modelling shows that conductivities lower than copper can be achieved in CNT/metal composites [4].

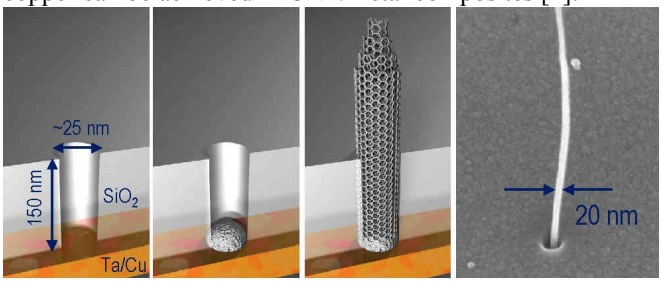

Fig. 2 Fabrication of end-of-the-roadmap sized MWCNT vias with ~20 nm in diameter and 150-200 nm in width. A 20 nm diameter multi-walled CNT is protruding from the via.

3. Transistors

Many of the problems that silicon transistor technology is or will be confronted with do not exist for CNT transistors. The strictly 1-dimensional transport in CNTs results in a reduced phase space, which enables almost ballistic transport and reduced scattering, especially at reduced gate length. The direct band structure of CNTs is completely symmetric for hole and electron transport and allows for symmetrical devices and optical active elements. As there are no dangling bonds in CNTs, the use of high-k material as gate dielectrics is simple. In fact, the application of Ta_xO_y, Hf_xO_y and Al_xOy as gate material have produced superior CNT transistors with low sub-threshold slopes and low hysteresis [6]. N-type and p-type doping is possible and can be performed by charge transfer from polymers or other polar species. It is not restricted to substitutional doping, which causes carrier scattering. CNTs are created in a "self-assembling" process and not by conventional top-down structuring methods. The scalability has been shown down to 18 nm channel length recently [7]. CNTs are chemically inert and due to the covalent bonds mechanically very stable. While all of these promising properties have been already verified on the laboratory scale, a detailed strategy for the large scale integration is still missing. Integrated CNTs have to fulfil a whole bunch of requirements simultaneously. The

most stringent demand being the precise placement of only semiconducting CNTs. The placement might be solved by localized growth of CNTs in vertical structures [1], as shown in Fig. 4, and the yield increase of semiconducting CNTs by special growth methods which favour the occurrence of only semiconducting CNTs [8]. But up to now, no one has devised a CNT device which incorporates all needs for a reliable switch.

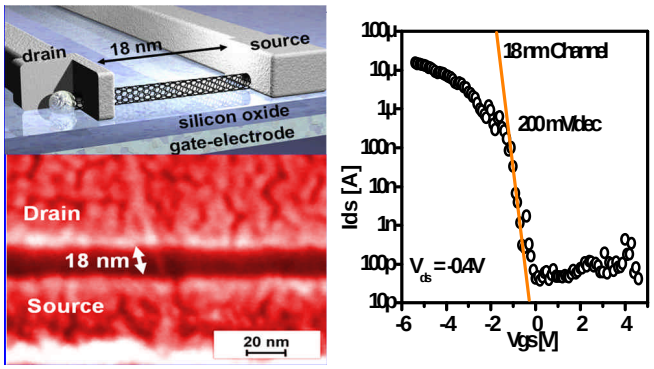

Fig. 3 A 18 nm channel length CNT transistor with 15 µA at 0.4 Volt on-current, showing no ambipolar behavior [7].

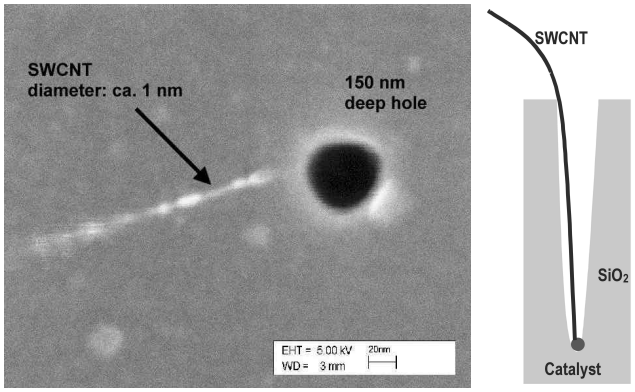

Fig. 4 Growth of a single-walled CNT in a precisely defined location.

4. Power transistors

Power switches are ubiquitous in use, need high blocking voltages and very low on-resistances. CNTs could even improve these power devices due to the following key advantages [9]:

First of all, the nanotube acts as a current limiter, because the current in one single-walled CNT is limited to ~25µA. This is in contrast to most silicon devices where overload leads to heat-up and avalanche-effect which destroy the device. Second, the specific resistivity of a long SWCNT is only one tenth of copper wire [10], which means that we can in principle construct a power device with an on-resistance similar to a copper wire. For normal Si-based devices the on-resistance is orders of magnitude higher and scales roughly with a power law of the form $V^{2.3}$ for the required blocking voltage. Third, the sustained current densities in CNTs are orders of magnitudes higher than in silicon or even copper. Therefore, CNTs would enable very compact low-loss power switches if thousands and millions could be paralleled, as indicated in Fig.5 to deliver an overall current up to some kA.

From integration point of view, there would be the advantage that no precise control of CNT arrangement on nanometer scale would be required. However, all metallic and small band-gap CNTs need to be removed either by selective burning or functionalization. A prototype with ~300 CNTs in parallel has been devised which was able to deliver up to 2.4 mA @ 1Volt. The device, sketched in Fig. 6, had enough power to operate small motors and LEDs.

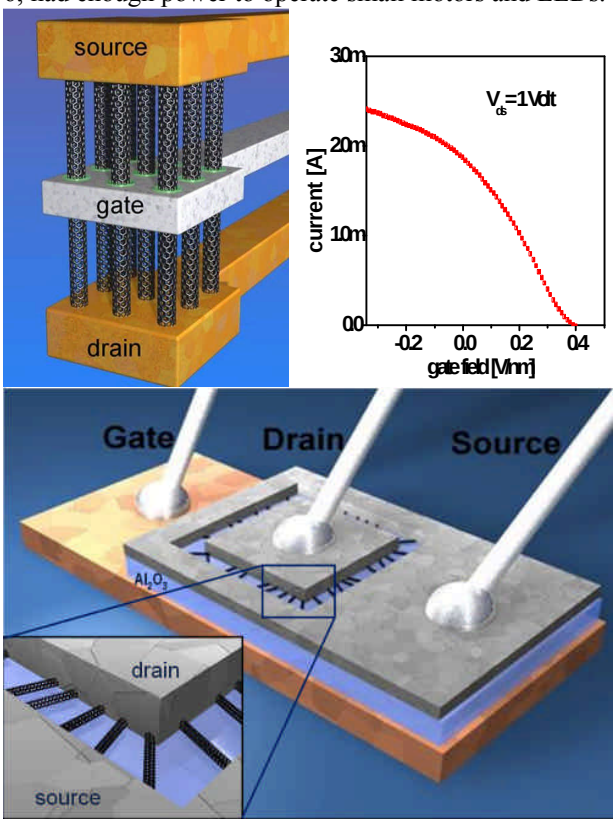

Fig. 5 Vertical CNT power transistor consisting of many nanotubes in parallel. A current of ~2.4 mA could be delivered with~ 300 paralleled tubes.

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References

(*) R. S. is now with AMD Dresden, Germany
[1] A. Graham et al., Small 1 (4): 382-390 APR 2005
[2] F. Kreupl et al., Microelectron. Eng. 64, p. 399-408 OCT 2002
[3] F. Kreupl et al., IEDM Tech. Dig. 2004
[4] O. Hjortstam, Appl. Phys. A., 2004; V.78, no.8, p.1175-1179
[5] M. Nihei et al., Proc. IITC 2005
[6] A. Graham et al., Appl. Phys. A 60 (6), 2004, p. 1141
[7] R. Seidel et al., Nano Letters 5 (1): 147-150 JAN 2005
[8] R. Seidel et al., J. Appl. Phys. 96 p. 6694, DEC 2004
[9] F. Kreupl et al. Patent pending 2003
[10] F. Kreupl et al., MRS Proceedings of AMC 2004, p. 285
[11] R. Seidel et al., Nano Letters 4 (5): 831-834 2004