



Design, Automation & Test in Europe
24-28 March, 2014 - Dresden, Germany

The European Event for Electronic
System Design & Test

Advancing CMOS with Carbon Electronics

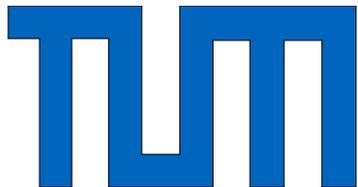
Prof. Dr. Franz Kreupl

Department of Hybrid Electronic Systems

Technische Universität München (TUM)

Munich, Germany

franz.kreupl@tum.de



Outline

- ❑ Introduction: The Quest for a New Logic Switch
- ❑ Graphene Nanoribbons or Carbon Nanotubes?
- ❑ **Consequences of missing current saturation in FETs**
- ❑ Disadvantages of Graphene Nanoribbons FETs
- ❑ Advantages of Carbon Nanotube Transistors
- ❑ Carbon Nanotubes as Tunneling FETS (TFET)
- ❑ The Big Challenge: How to make them

The Quest for a New Logic Switch

□ Key drivers

- enhanced drive current
- lower power
- better electrostatics
- variability

mobile application

materials /contacts

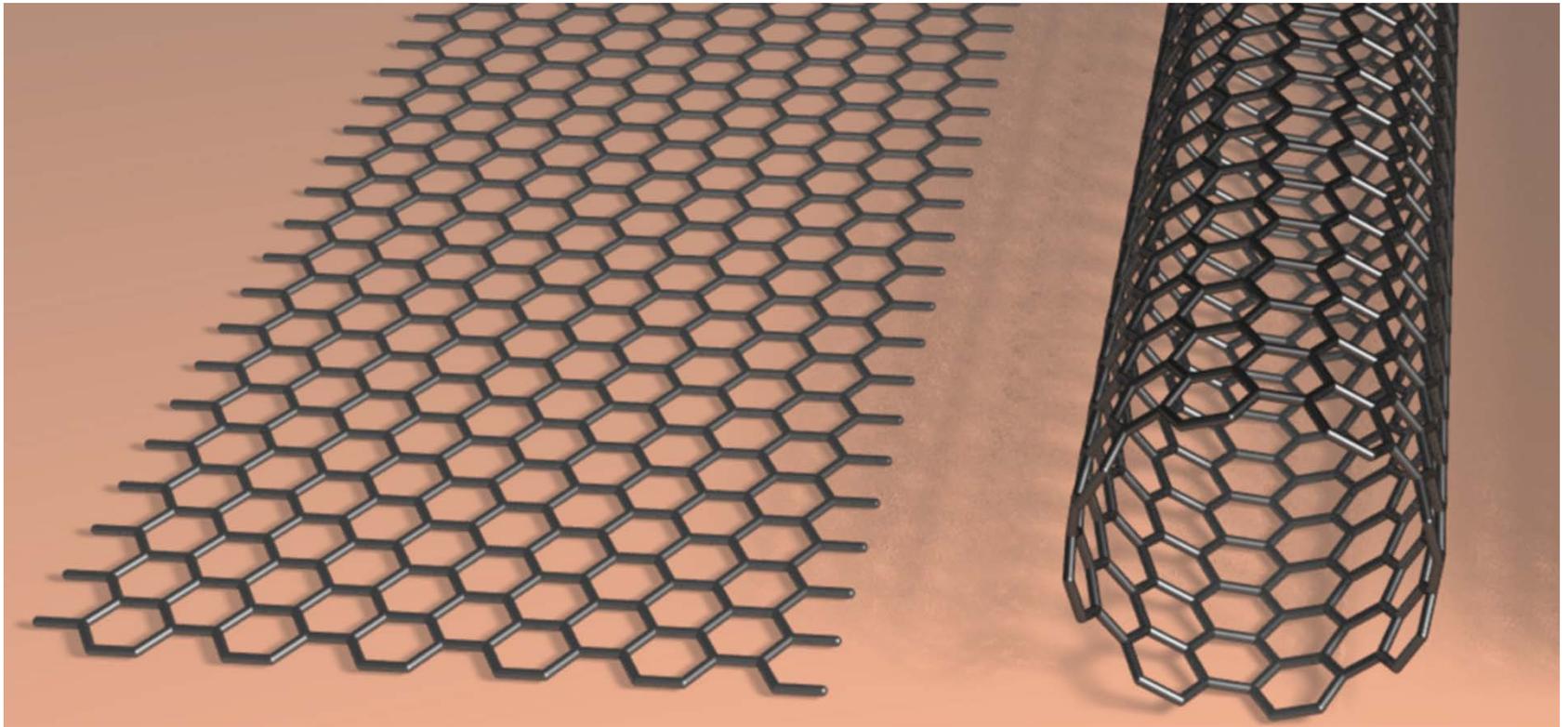
low voltage /leakage

gate-all-around

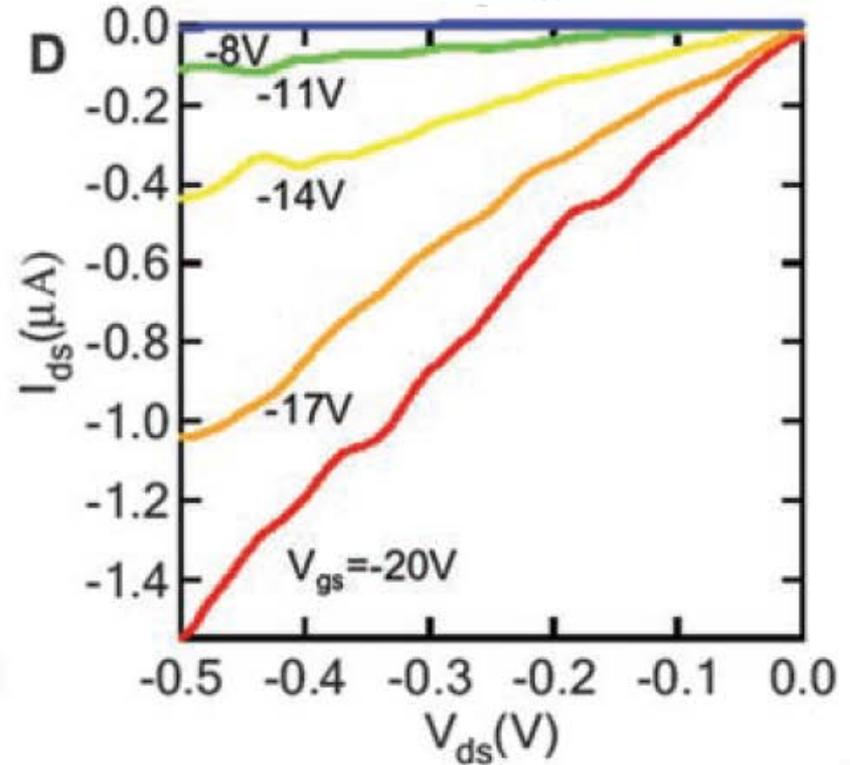
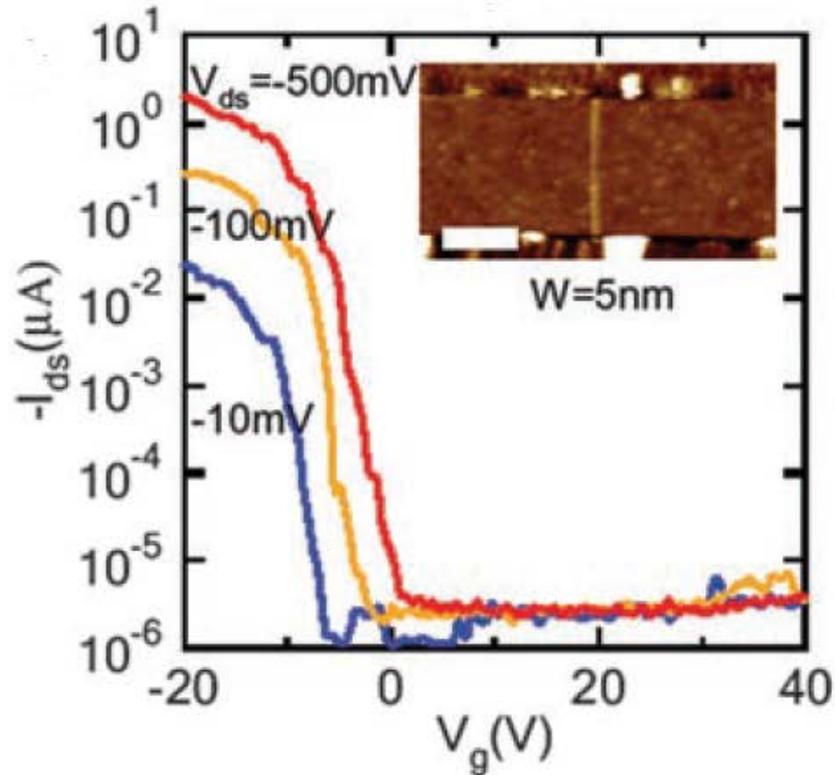
no doping

Graphene Nanoribbons or Carbon Nanotubes ?

- ❑ Leading candidates for high mobility materials
- ❑ Graphene (ribbons) or single-walled carbon nanotubes

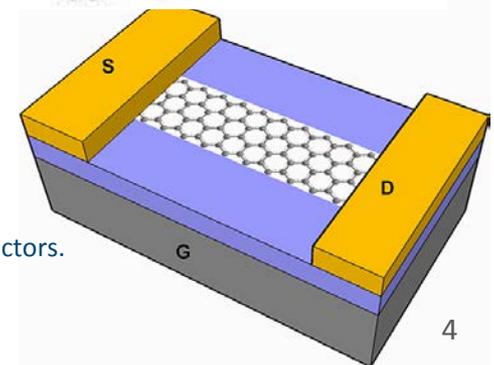


Graphene nanoribbon do have band gap



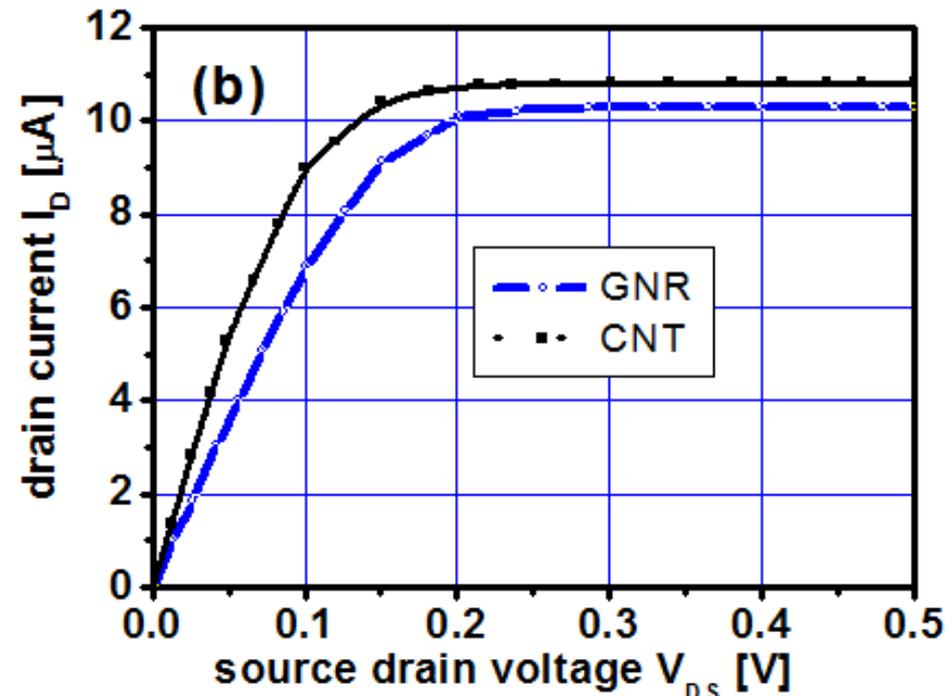
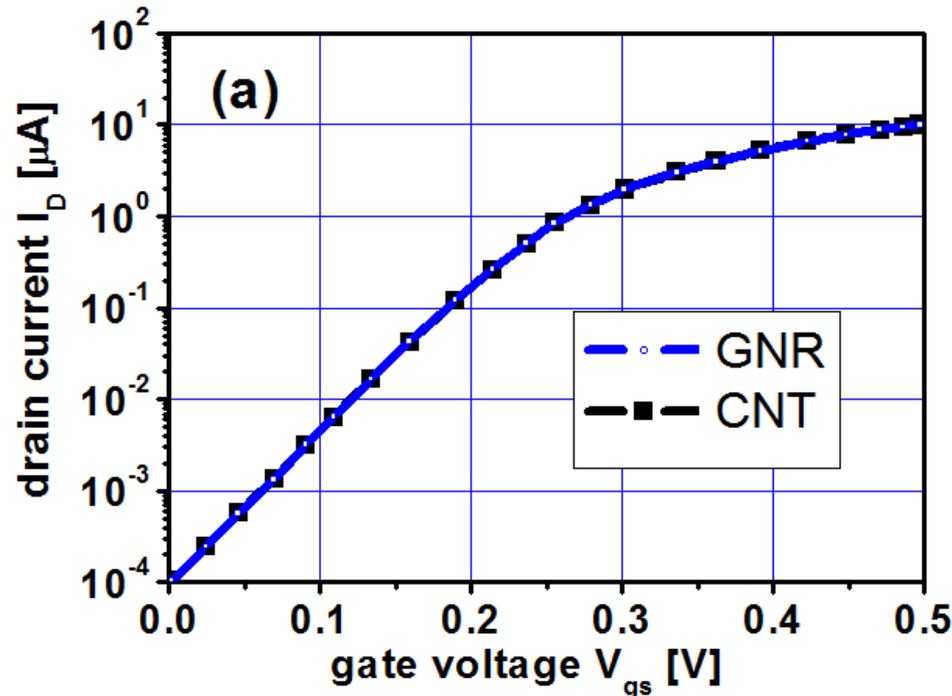
- ❑ band gap introduction leads to mobility loss
- ❑ device can be turned off

Li, X., Wang, X., Zhang, L., Lee, S. & Dai, H. Chemically derived, ultrasmooth graphene nanoribbon semiconductors. Science 319, 1229–1232 (2008)



Graphene (GNR) versus Carbon Nanotubes

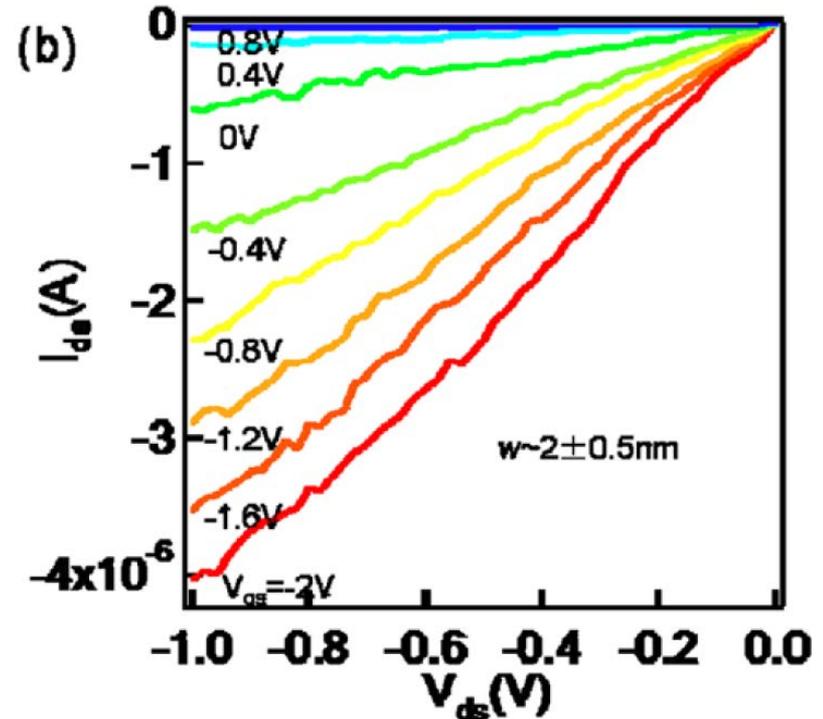
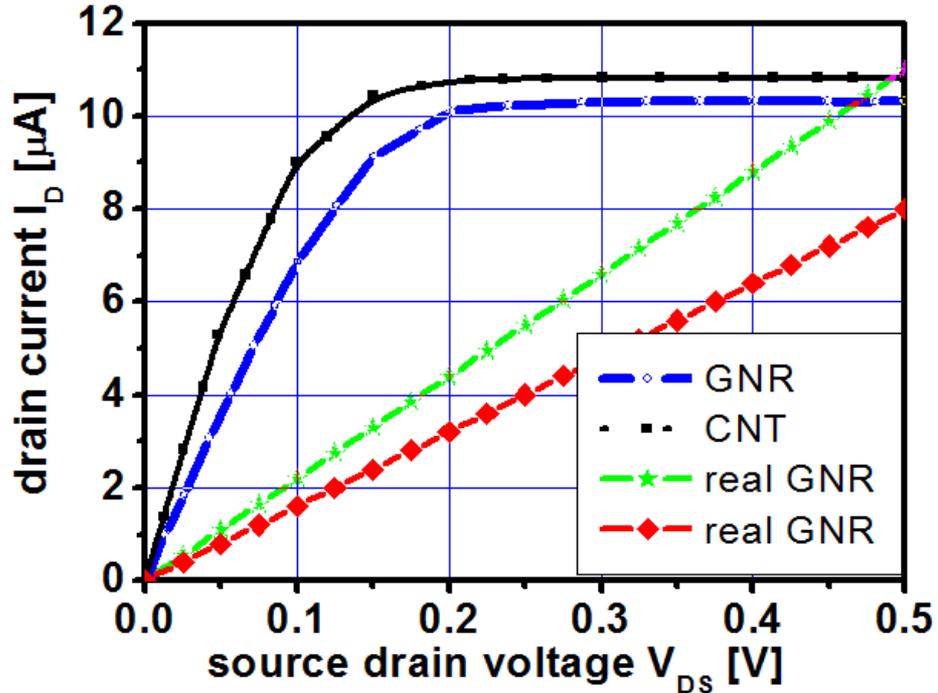
data taken from: Y. Ouyang, Y. Yoon, J. K. Fodor, J. Guo, "Comparison of performance limits for carbon nanoribbon and carbon nanotube transistors", Appl. Phys. Lett. 89, 203107 (2006).



- almost no difference between GNR and CNTs in simulation
- both show excellent FET behavior at low voltages
with current saturation
- GNR with bandgap should solve the problem that CNT have!

Graphene (GNR) vs. Carbon Nanotubes

real GNR do not show current saturation

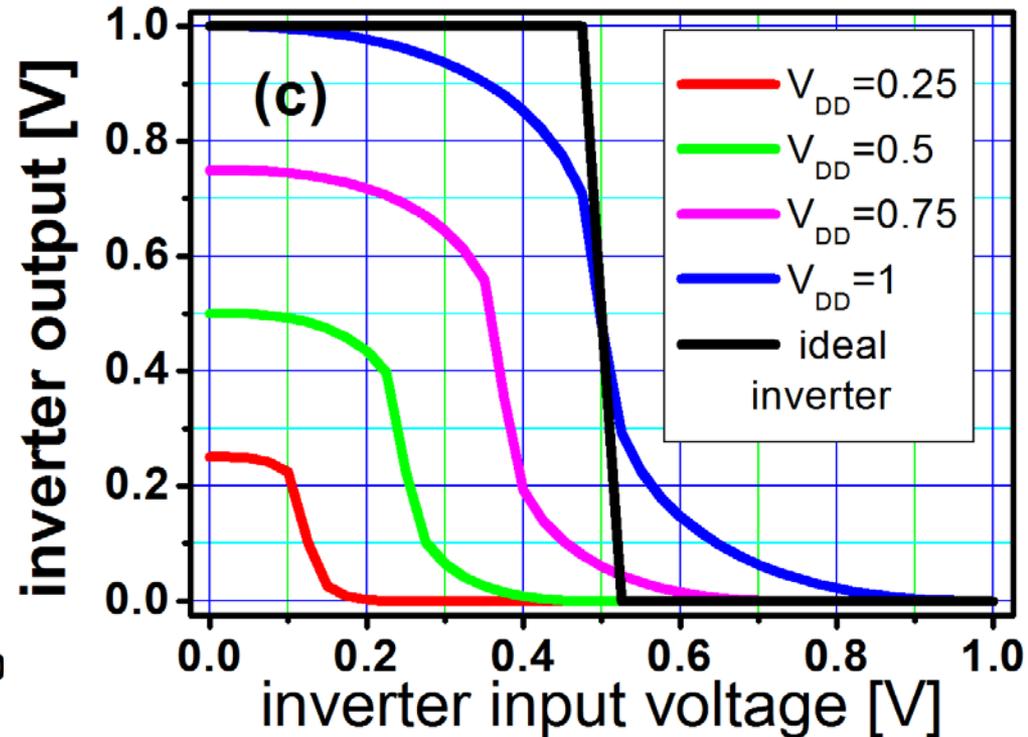
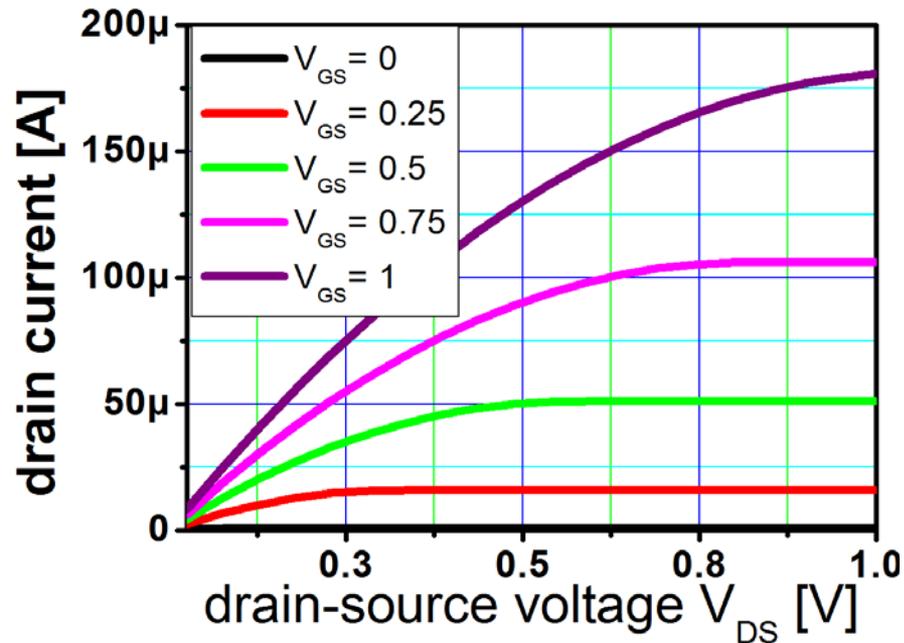


- real GNR exhibit a linear dependence of I_D on V_{DS}
- current saturation is only observed at **long gate length**
high V_{DS} and high current density

X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, "Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors", Phys. Rev. Lett. 100, 206803 (2008).

Transistors with current saturation

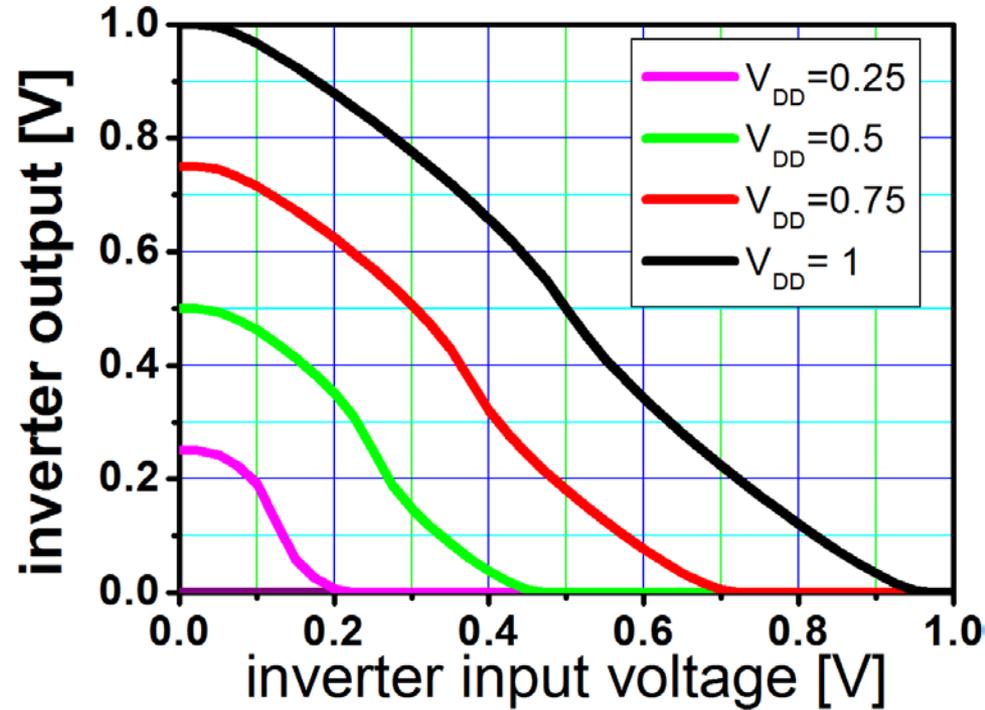
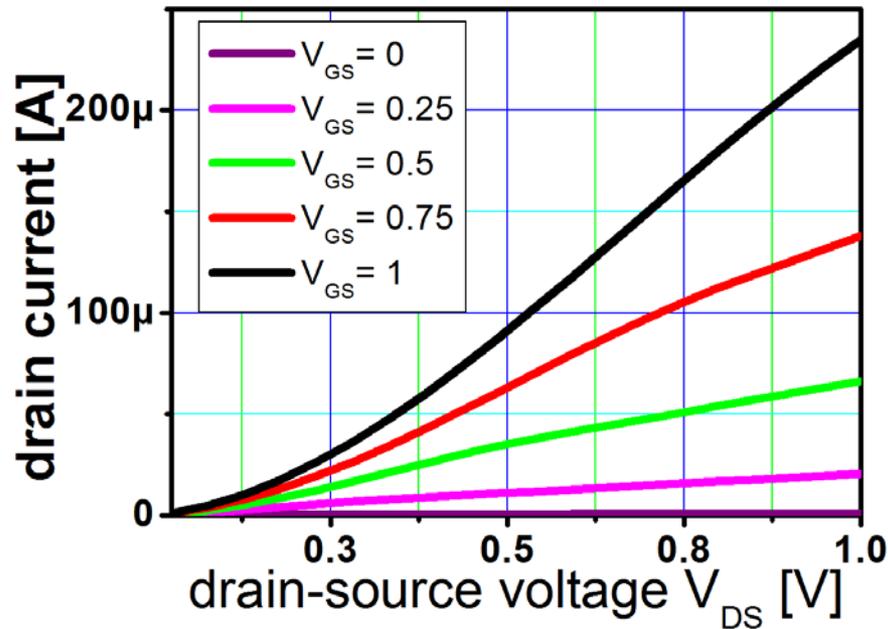
Effect on Inverter



- absolute gain $\gg 1$ at $V_{DD}/2$
- sharp transitions for cascaded logic
- useful for SRAM, sense amp etc..

Transistors without current saturation

Effect on Inverter



- absolute gain only ~ 1 at $V_{DD}/2$
- no noise immunity, burns constantly current
- no sharp transitions for cascaded logic
- not useful for logic, SRAM or latch-type sense amp etc..

Graphene transistors: bad devices

**even graphene nanoribbon transistors
(which do have a band gap)**

failed to show:

**current saturation @ low voltage and
@ short gate length**

Therefore: no voltage gain = bad RF-FET

low gain inverters = bad logic-FET

nice overview article for RF devices:

Frank Schwierz:

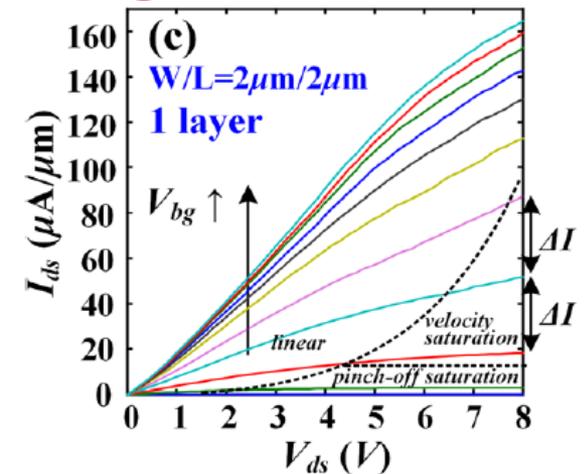
Graphene Transistors: Status, Prospects, and Problems

Proceedings of the IEEE Vol. 101, No. 7, July 2013

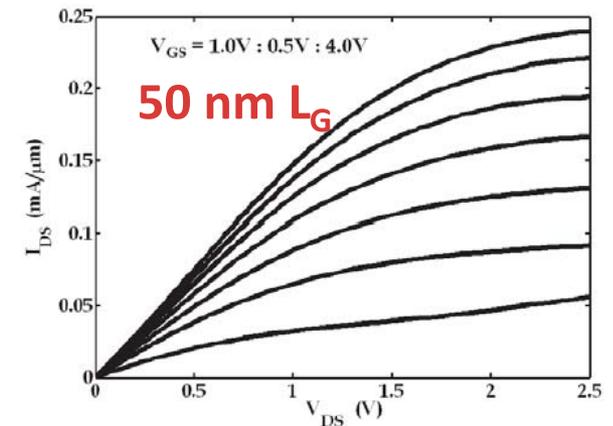
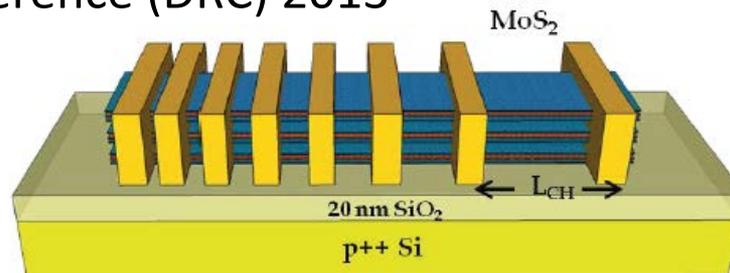
... same for MoS₂ transistors (& other 2D)

no current saturation @ low voltage and
@ short gate length

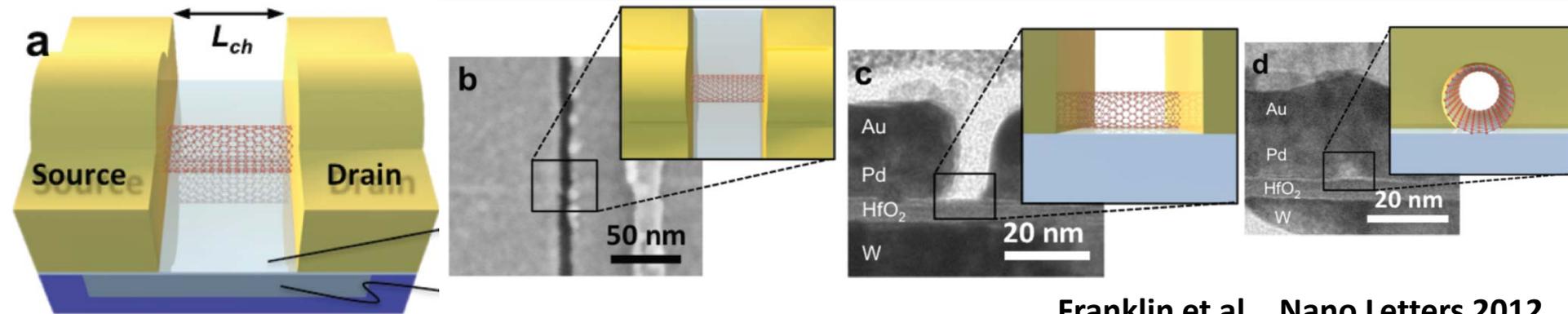
High-performance MoS₂ transistors with low-resistance molybdenum contacts, Kang, Liu, and Banerjee
Appl. Phys. Lett. 104, 093106 (2014)



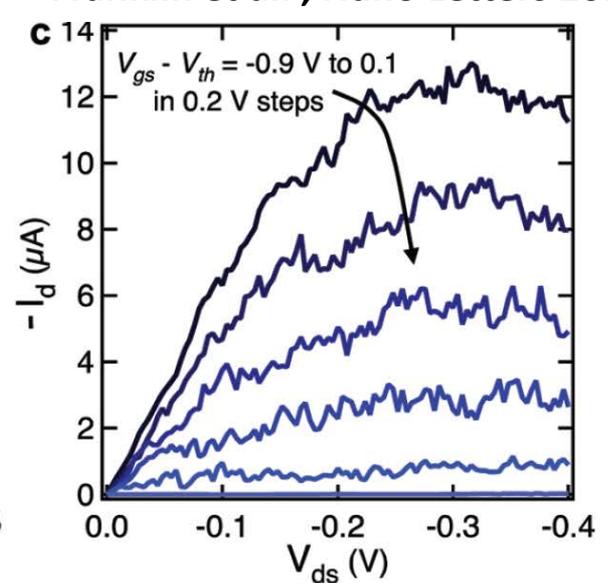
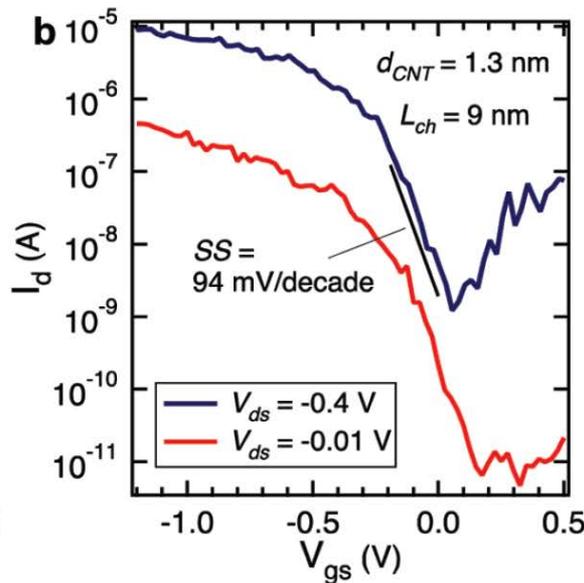
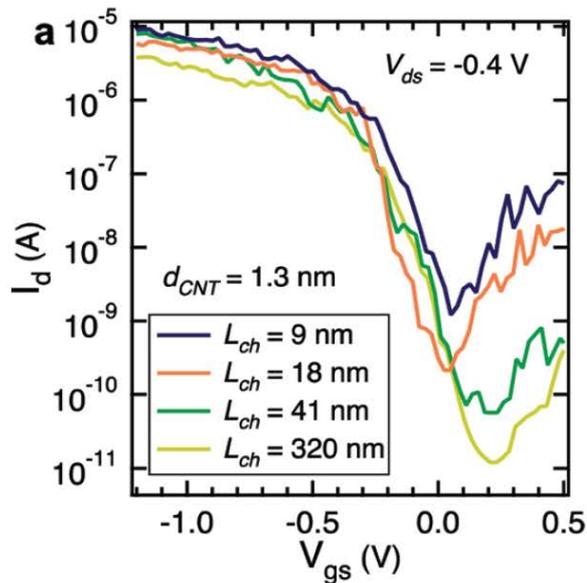
Evaluating the scalability of multilayer MoS₂ transistors
S. Das, J. Appenzeller
Device Research Conference (DRC) 2013



Sub-10 nm carbon nanotube transistor



Franklin et al. , Nano Letters 2012



Operation at low V_{DS} (0.4V) and short L_{gate} of 9 nm

A. D. Franklin, M. Luisier, S.J. Han, G. Tulevski, C.M. Breslin, L. Gignac, M.S. Lundstrom, W. Haensch, "Sub-10 nm Carbon Nanotube Transistor", Nano Lett., 12 (2), 758–762 (2012). F. Kreupl, Nature 484, 321–322 (2012)

Advantages of Carbon Nanotubes FETs

Carbon Nanotubes fulfill our wishlist for a new switch

❑ Gate-all-around structure

work: Franklin et al. , IEDM 2012

patent: Kreupl & Seidel US 7646045 B2

❑ No/low DIBL, very high on-current

❑ Doping-free for reduced variability

❑ Metallic, scalable source/drain contacts

❑ ~6 kOhm for a 1 nm wide channel! Franklin et al, Nature Nanotech. 2010

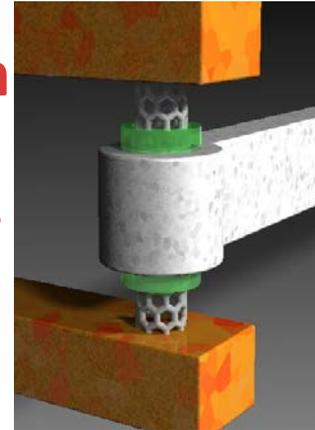
❑ Compatibility with high-k materials

❑ LaOx, HfOx, ZrOx, TaOx, AlOx, TiOx all work

❑ Scalability demonstrated down to 9 nm Franklin et al. , Nano Letters 2012

❑ short L_G data is not available for InGaAs, Ge, GeSn, SiGe....

❑ dark space might worsen situation for InGaAs, Ge, GeSn

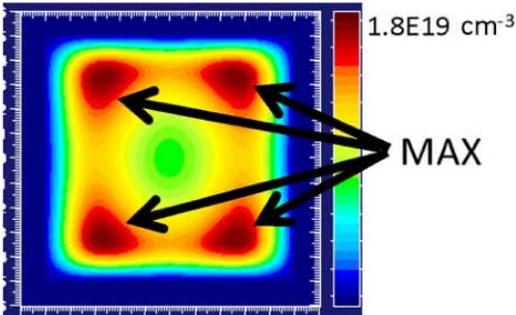


Kreupl, IFX 2003

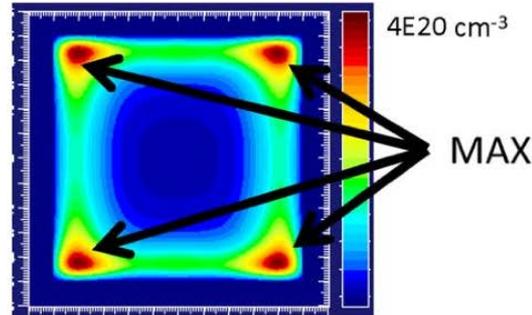
http://www.hes.ei.tum.de/fileadmin/w00bjl/www/uploads/Kreupl_New_materials_on_horizon_for_advanced_logic.pdf

Dark space in silicon / high- μ channels

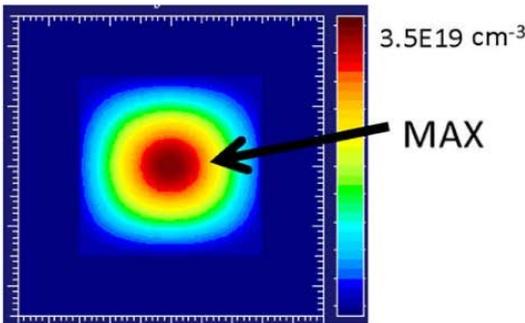
10 nm wire, low field



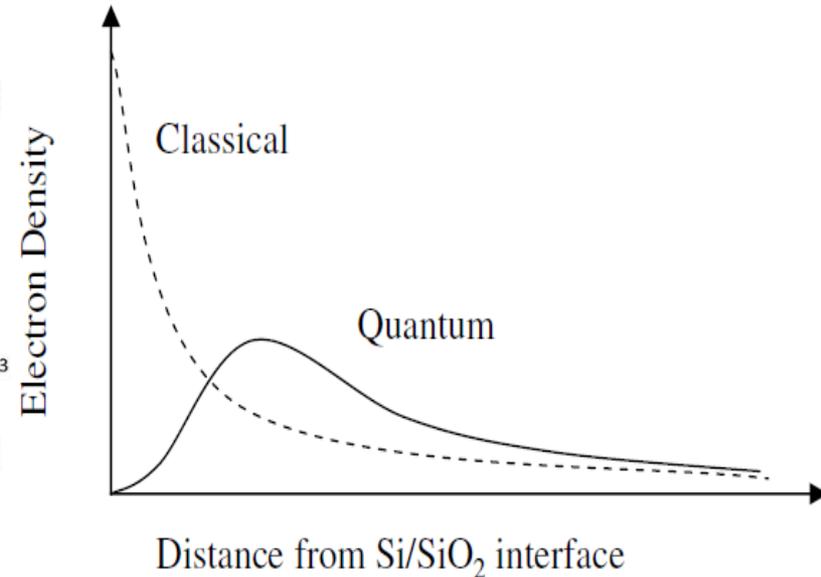
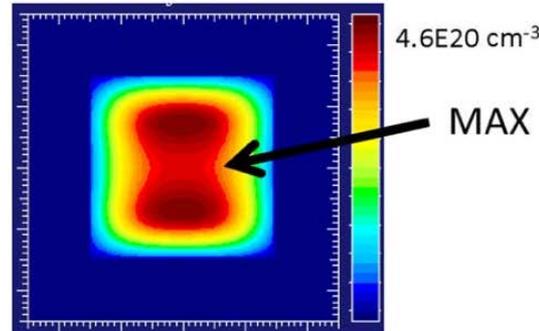
10 nm wire, high field



3 nm wire, low field



3 nm wire, high field



in Silicon Kelin J. Kuhn, TED 2012

- ❑ Dark space gets worse due to reduced DOS – $C_{inv} \propto 1/\text{DOS}$
- ❑ No matter how high the k-value \rightarrow dark space destroys it
- ❑ Severe limiter for channel control \rightarrow SS / DIBL deterioration

Skotnicki & Boeuf, VLSI 2010

Ge-, InAs-Scaling – dark space

25 nm Germanium Quantum Well pMOS FinFETs

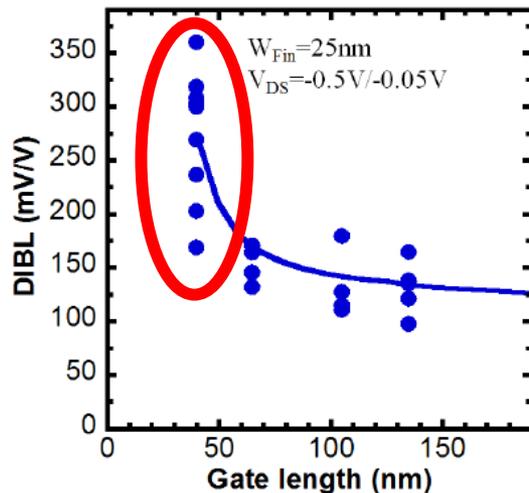


Fig. 12. DIBL versus L_G for sGe/SiGe Fin devices. Electrostatics are not significantly degraded with L_G scaling down to ~ 65 nm due to the additional isolation from the quantum barrier between sGe and SiGe SRB

L. Witters et al. IMEC, IEDM 2013

No data on SS @ short L_G
Why?

Severe limiter for channel control \rightarrow SS / DIBL deterioration Skotnicki & Boeuf, VLSI 2010

20 nm InAs-on-insulator Tri-gate

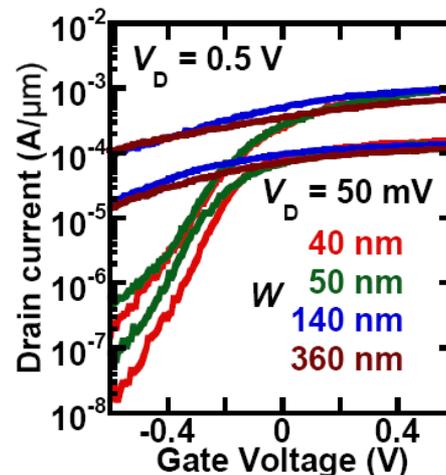


Fig. 14 W dependence of transfer characteristics at $L_{ch} = 20$ nm.

SangHyeon Kim et al., Tokyo U, IEDM 2013

some data only at 150 K
Why?

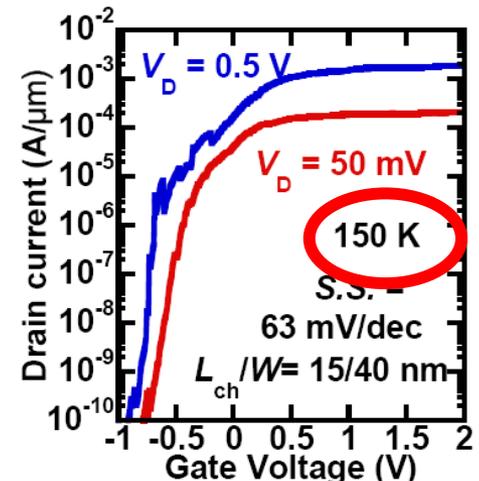
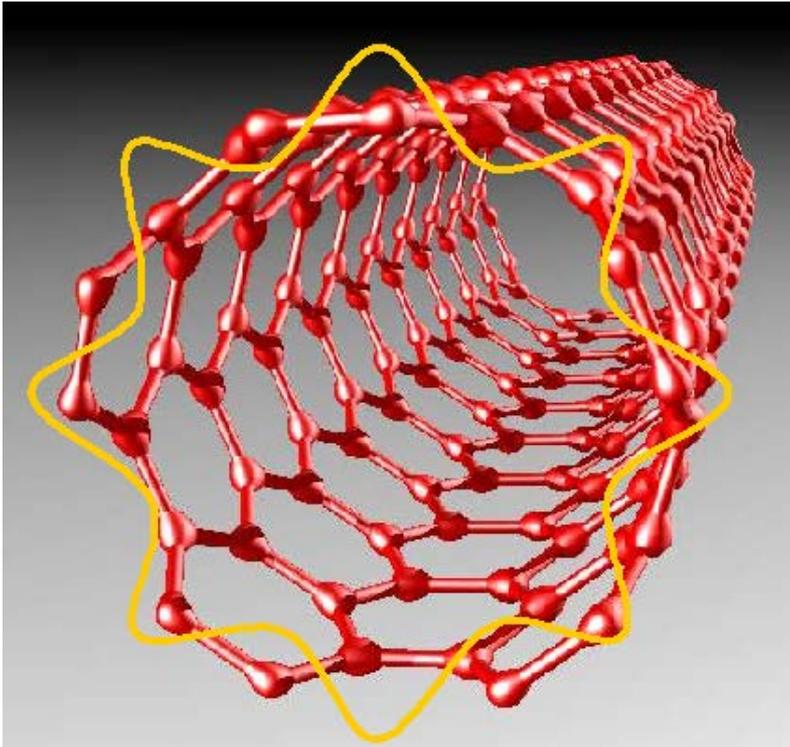


Fig. 15 Transfer characteristics of InAs-OI MOSFETs with $L_{ch}/W = 15/40$ nm at 150 K.

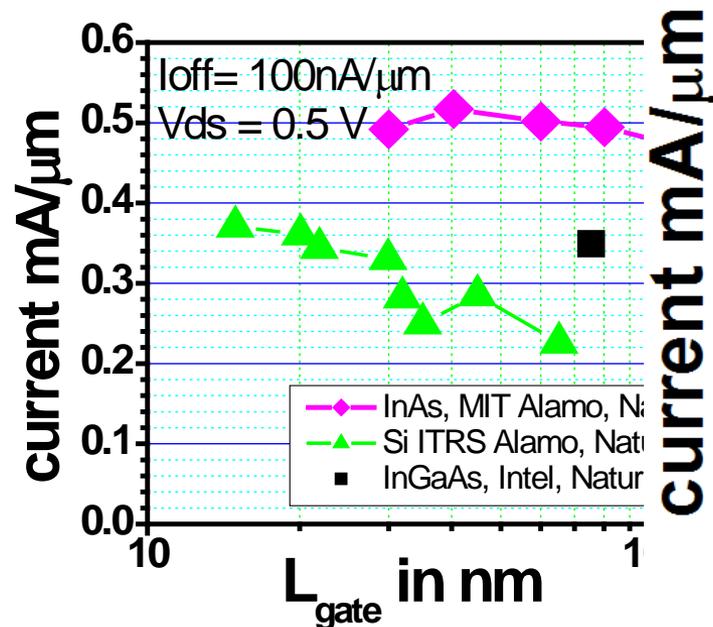
Carbon Nanotubes have no dark space



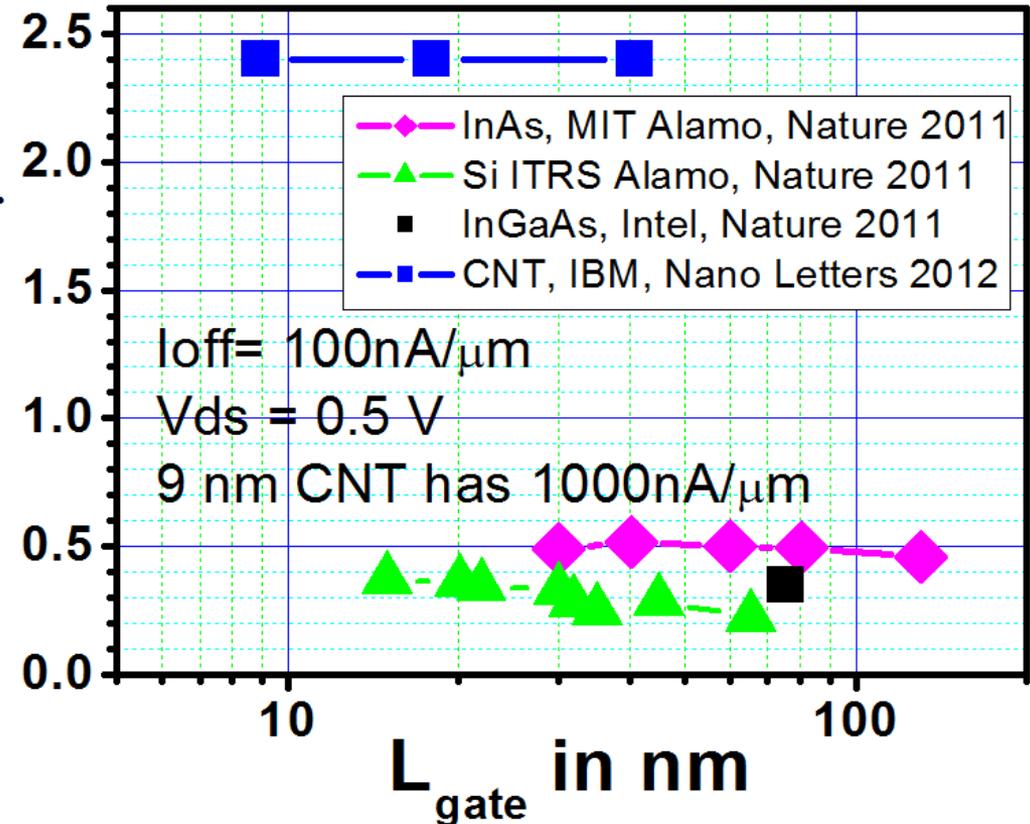
- ❑ Current is confined to a single atomic layer
- ❑ Intimate channel control & low DOS
- ❑ Operation in the quantum capacitance limit (QCL) possible
- ❑ In QCL, the potential in channel is determined by the gate potential
- ❑ short channel effects are suppressed
- ❑ Nanotube have no dopants

c.f. Knoch et al. EDL, 2008

Carbon nanotubes outperform alternatives



Jesus Alamo, Nature 2011

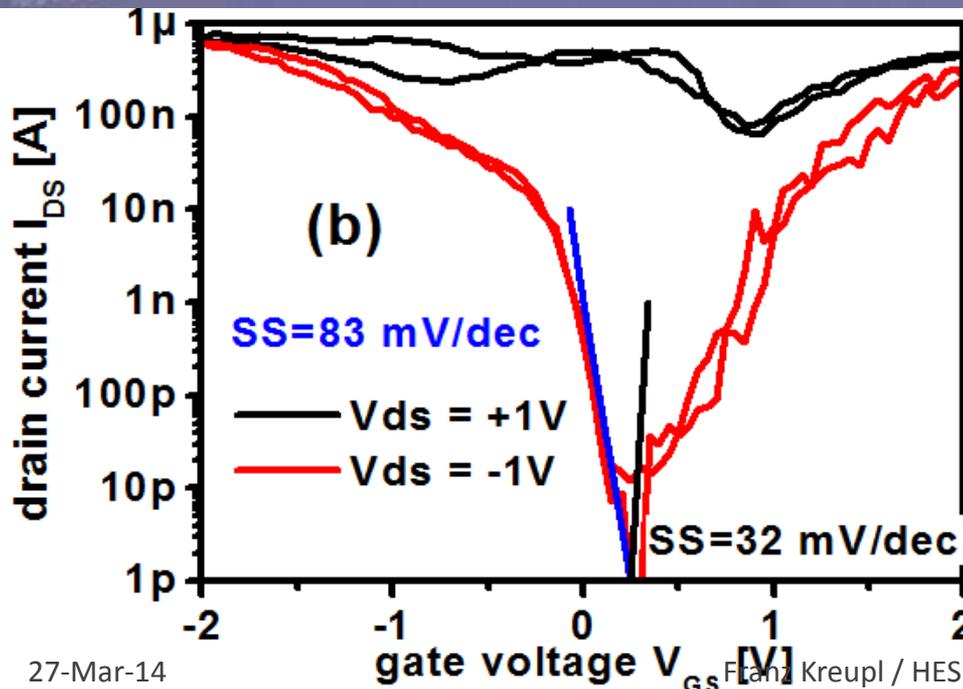
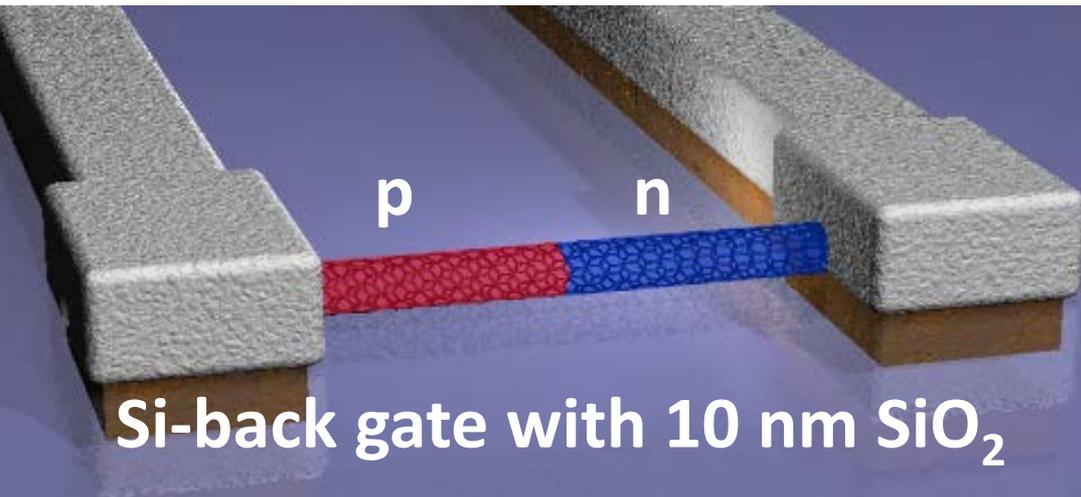


enhanced current drive due to material and contacts

F. Kreupl, Nature 484, 321–322 (2012)

CNT I_{off} : 1000 nA/μm for 9 nm !
100 nA/μm for ≥ 18 nm

Carbon Nanotubes Tunneling FETs (TFET)



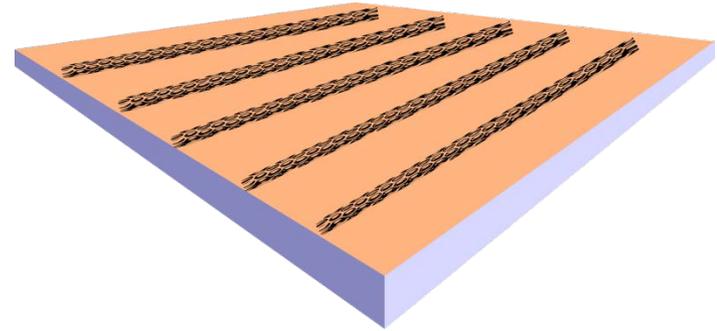
- gated PIN diode based on a CNTFET
- n-doping by PEI polymer
- p-doped by contacts & atmosphere
- SS of 83 mV/dec and current drive of $\sim 1\text{mA}/\mu\text{m}$
- unknown doping profile
- E field sharper by local screening gates?

F. Kreupl, "Carbon Nanotubes in Microelectronic Applications", in Advanced Micro & Nanosystems Vol. 8. Carbon Nanotube Devices, edited by Christofer Hierold, WILEY-VCH (2008)

Great News – how to proceed?

Please give instructions

- ➔ how to place **billions** of nanotubes with
- one type of **chirality**
 - equal **length**
 - on a substrate
 - well aligned at some **nanometer pitch**
 - with a **throughput of 120 wafers per hour**



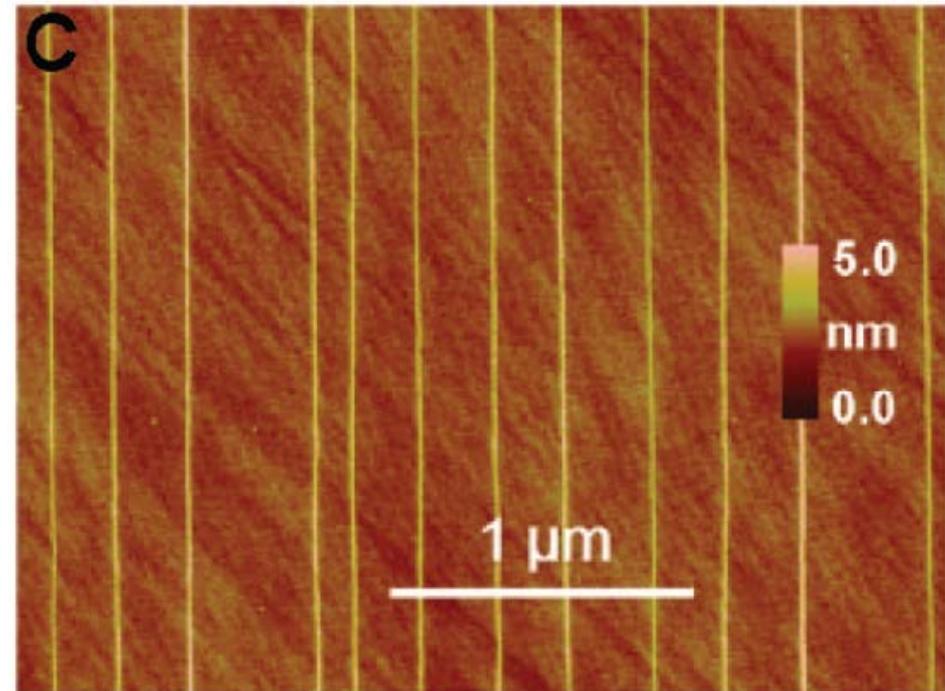
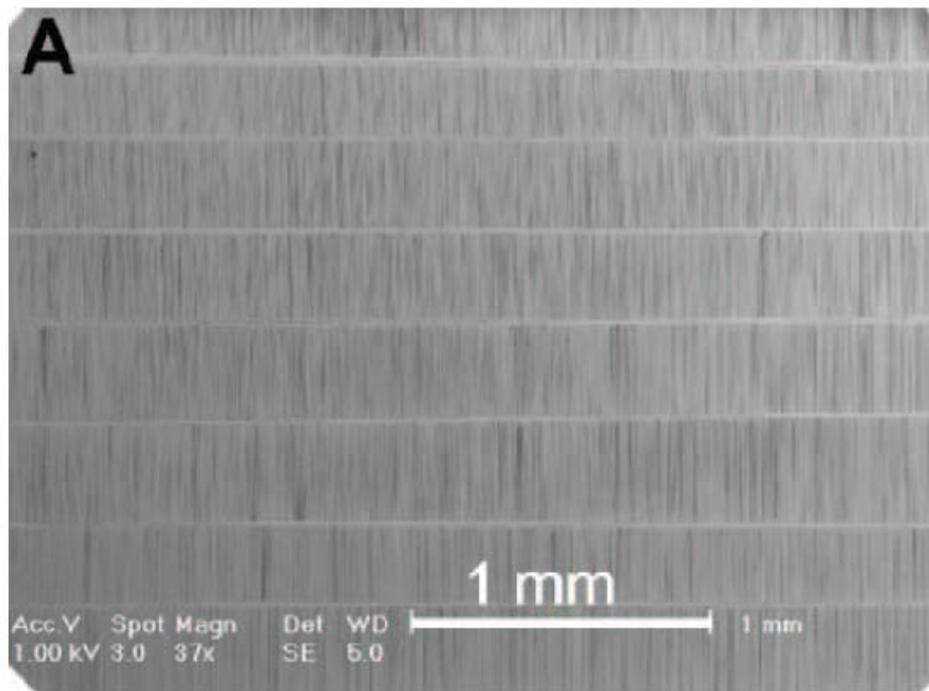
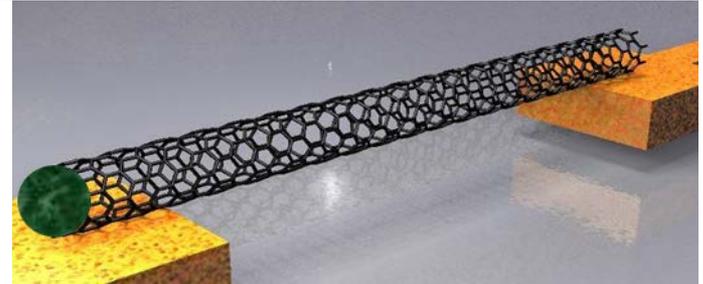
Solution: Just issue a purchase order for the new Applied Materials *Nano-Wonder™* machine

No - unfortunately – I am kidding



Placement strategies are to be investigated

- Grow **in place** or **transfer**
- Use **self-assembly**



- aligned growth is possible, pitch not (yet) suitable**

(Selective Growth of Well-Aligned Semiconducting Single-Walled Carbon Nanotubes

Lei Ding, Alexander Tselev, Jinyong Wang, Dongning Yuan, Haibin Chu, Thomas P. McNicholas, Yan Li, and Jie Liu

27-Mar-14 Nano Lett., 2009 DOI: 10.1021/nl803496s Franz Kreupl / HES TUM

Summery and Conclusion

- ❑ There is **no single experimental evidence** that Graphene and other 2D materials are suitable for further scaling of FETs
- ❑ The main culprit is **missing current saturation**
- ❑ Opportunity **window for alternative channel materials** is **closing** due to **dark space** effects
- ❑ Performance-wise carbon **nanotube devices outperform** any alternative
- ❑ **Huge gap** for industrial **integration** exists
- ❑ A **possible roadmap exists** based on **self-assembly** and/or **grow in place**
- ❑ What remains is **hard work to make it happen** – not ideally suited for academia