Carbon-based Materials as Key-Enabler for "More-than-Moore" Devices

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Outline

Carbon FET Devices

- Carbon Nanotubes
- Challenges

Carbon Interconnects

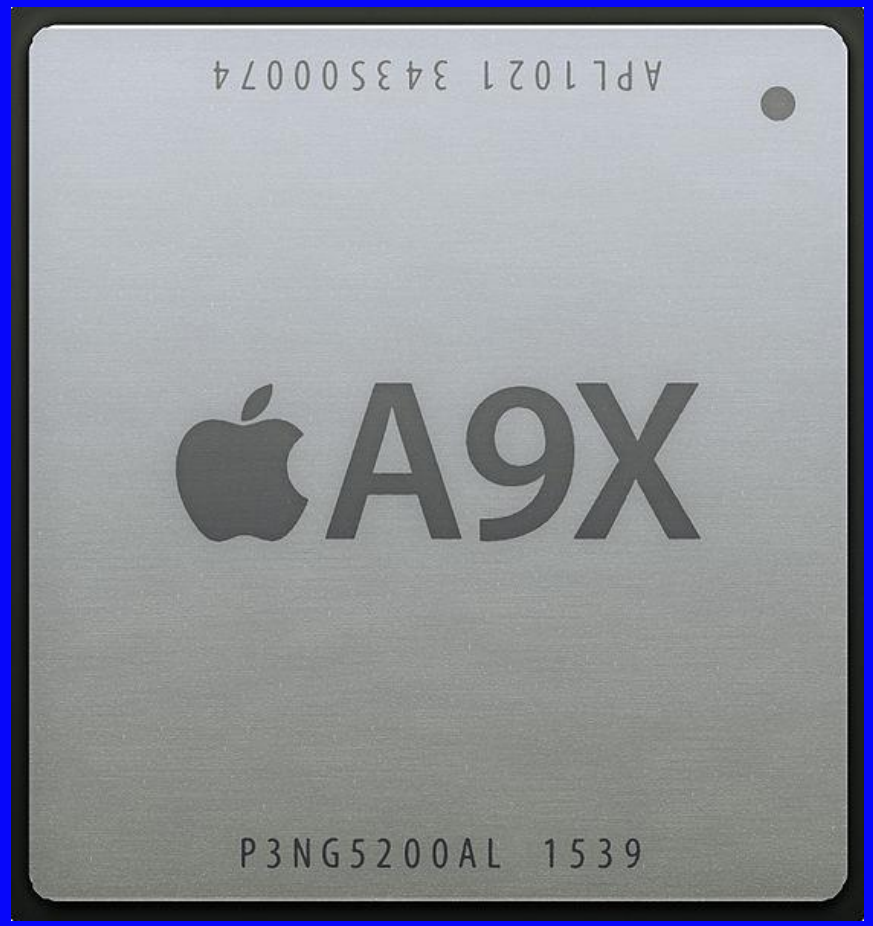
- Thru Silicon Vias
- DRAM Capacitors
- Carbon-Silicon Schottky Diodes

Graphenic Carbon Membranes

- X-ray Transmission Windows
- Carbon-based Resistive Memories
- Photodetectors
- Carbon-based Spin-Filters

Computation Power

345.6 GFLOPS



368.2 GFLOPS

Hitachi CP-PACS/2048
best supercomputer in 1996

Moore's law rewritten

Why scaling makes sense

Energy E to change a logic level

$$E = C V^2$$

- V → voltage
- C → capacitance = dimension, scale

few electron logic possible

next level: interconnect reduction

Lower Capacitance per Function

Mark Bohr (Intel):
"…… We make sure we're **scaling the capacitance** per transistor or **capacitance per function**. So you get that switch energy benefit."

Interview with Mark Bohr from August 22, 2016 with Mark Lapedus
http://semiengineering.com/deeper-inside-intel/

Why scaling makes sense

Moore's law rewritten

Time delay **τ** to change a logic level:

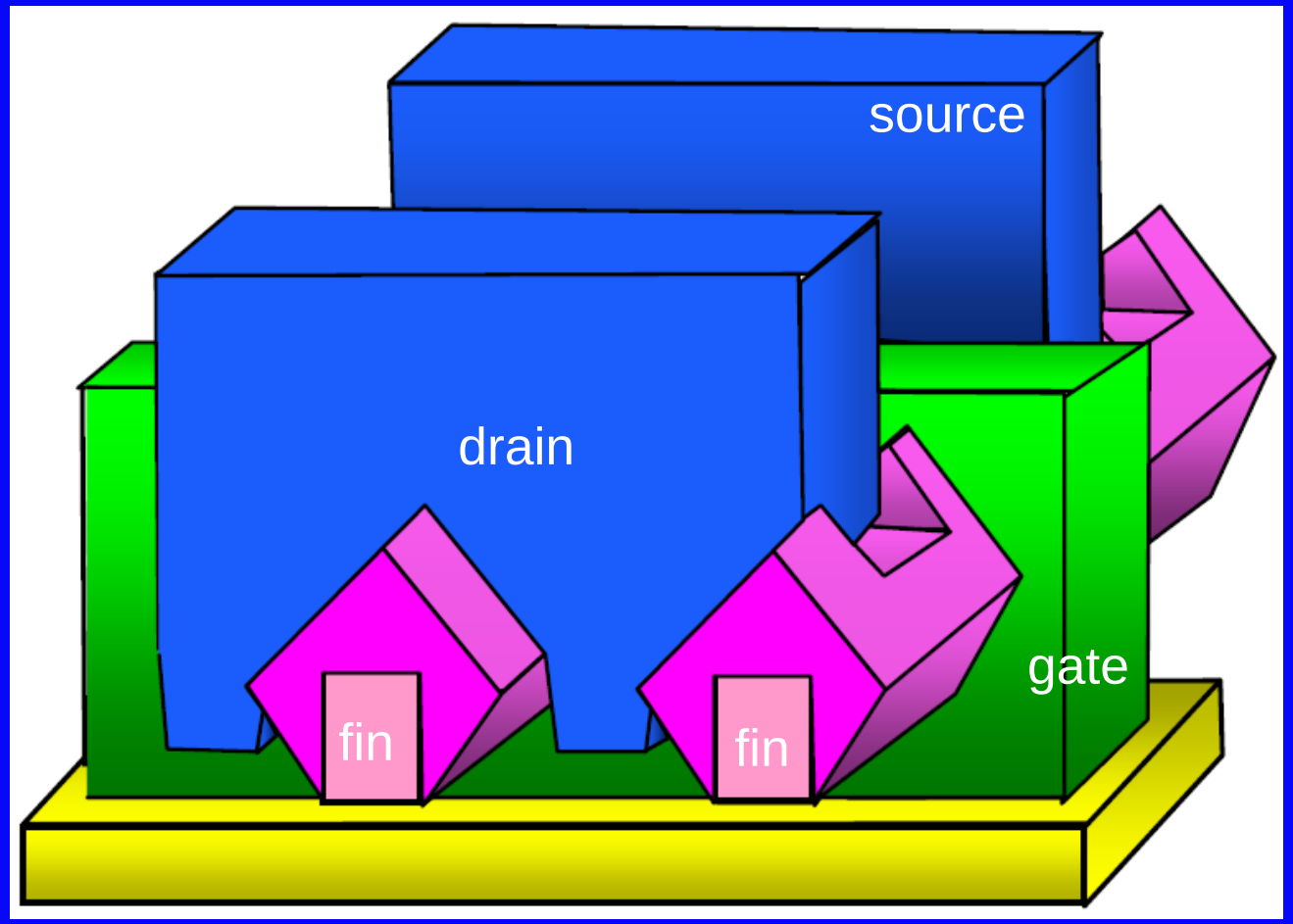
$$\tau = \frac{C \cdot V}{I_{ON}}$$

I_{ON} → Current drive of the switch

Device physics determines I_{on}

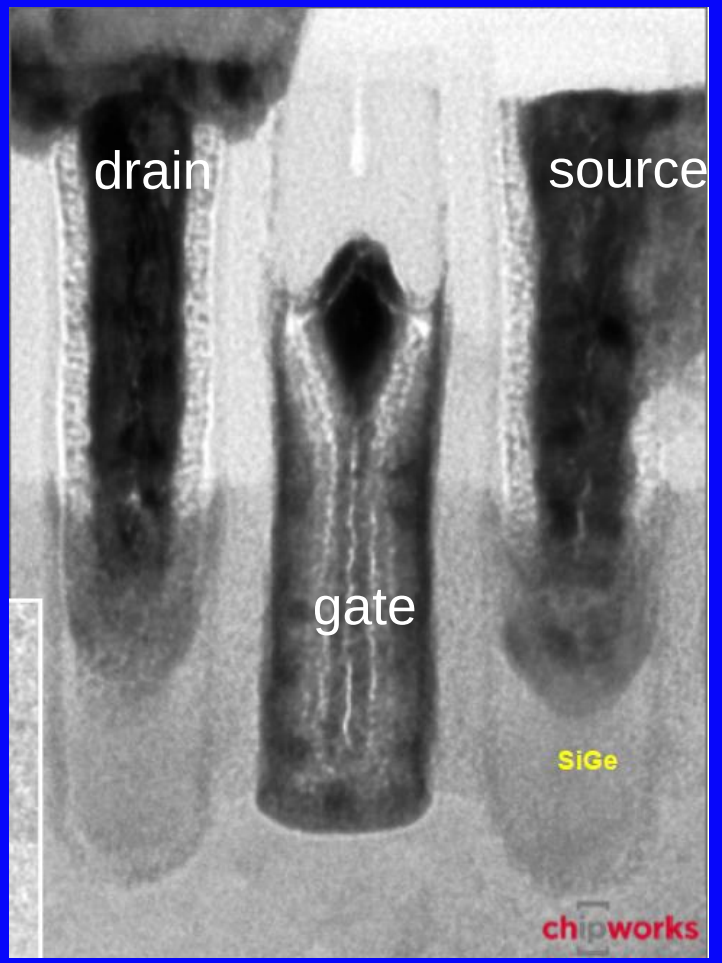
Geometry determines **C**

When scaling makes NO sense



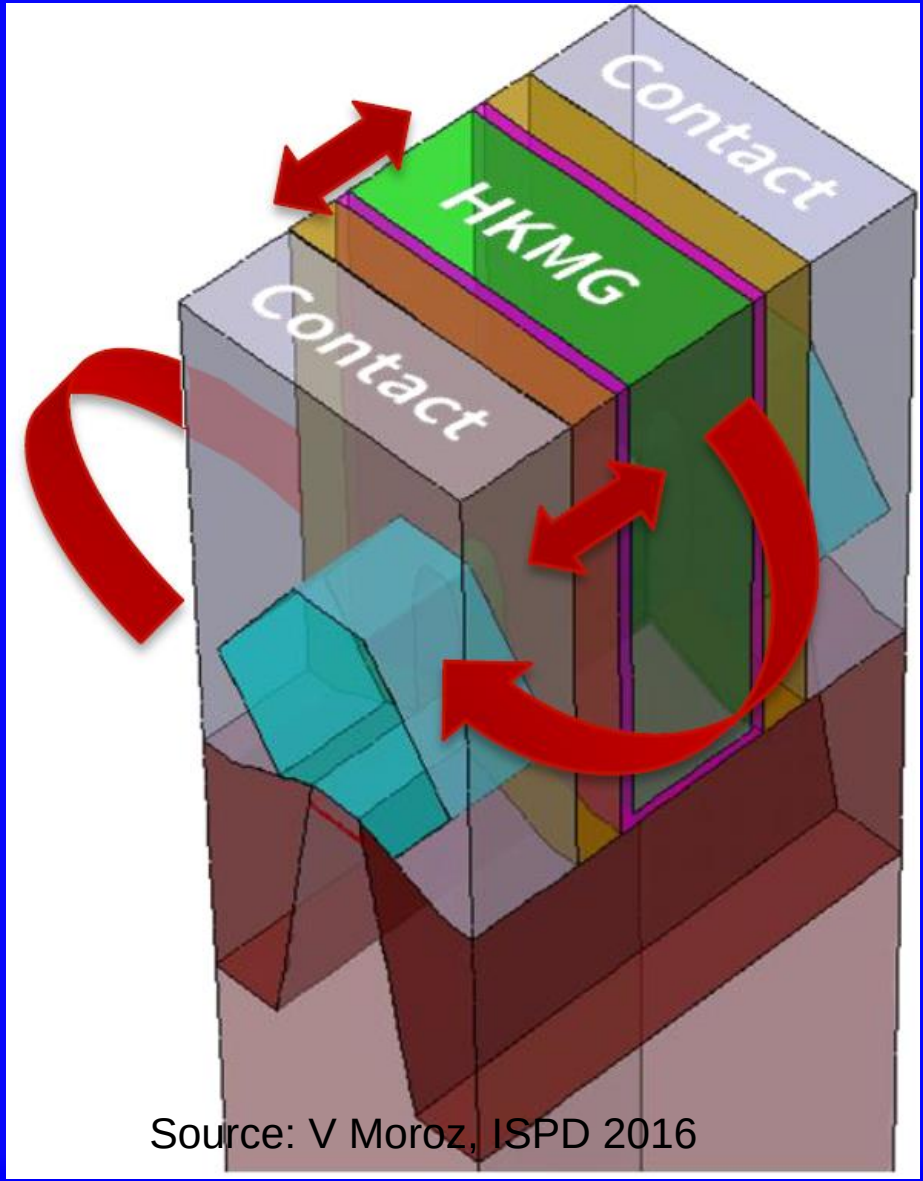
Source: Kuhn, IEDM 2008

Intel 14 nm Trigate

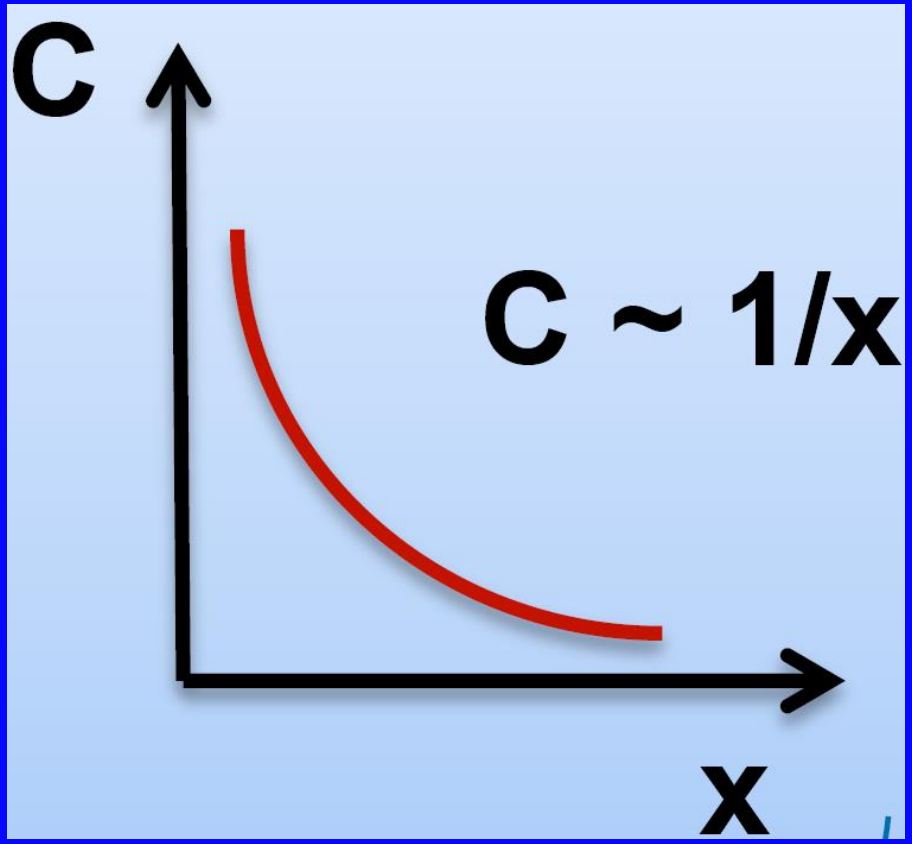


Source: Dick James, 2015

When scaling makes NO sense



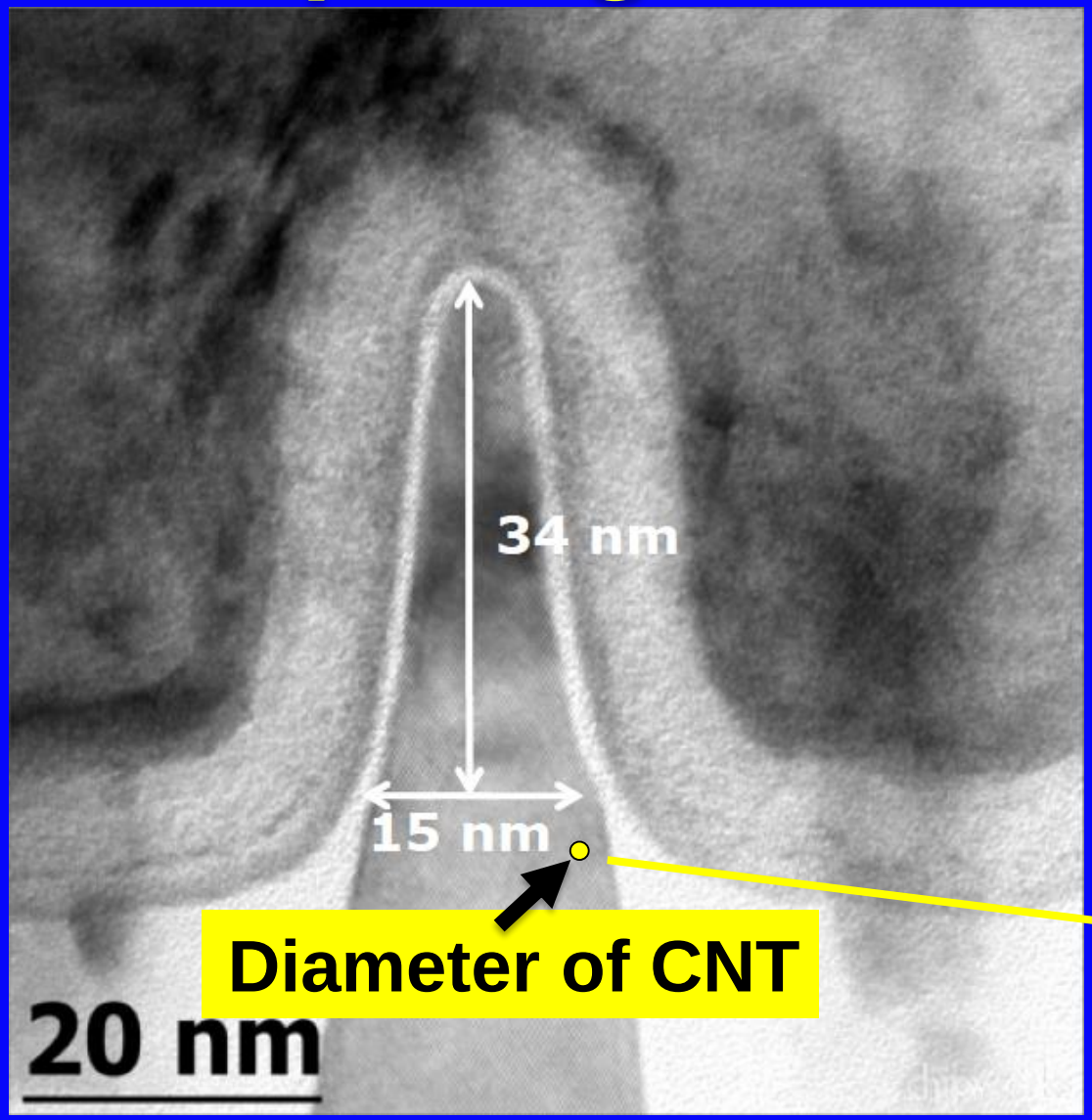
Source: V Moroz, ISPD 2016

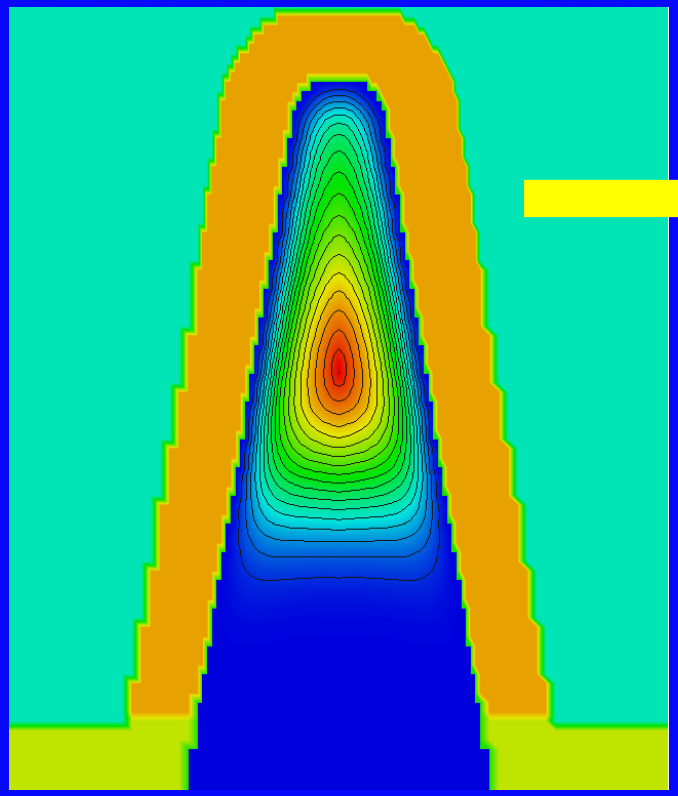


Increase of

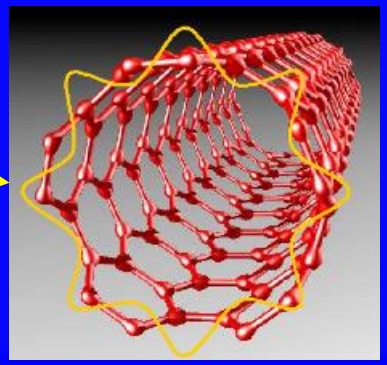
- **stray capacitance**
- **middle of line capacitance**

Comparing FinFet with Carbon Nanotube





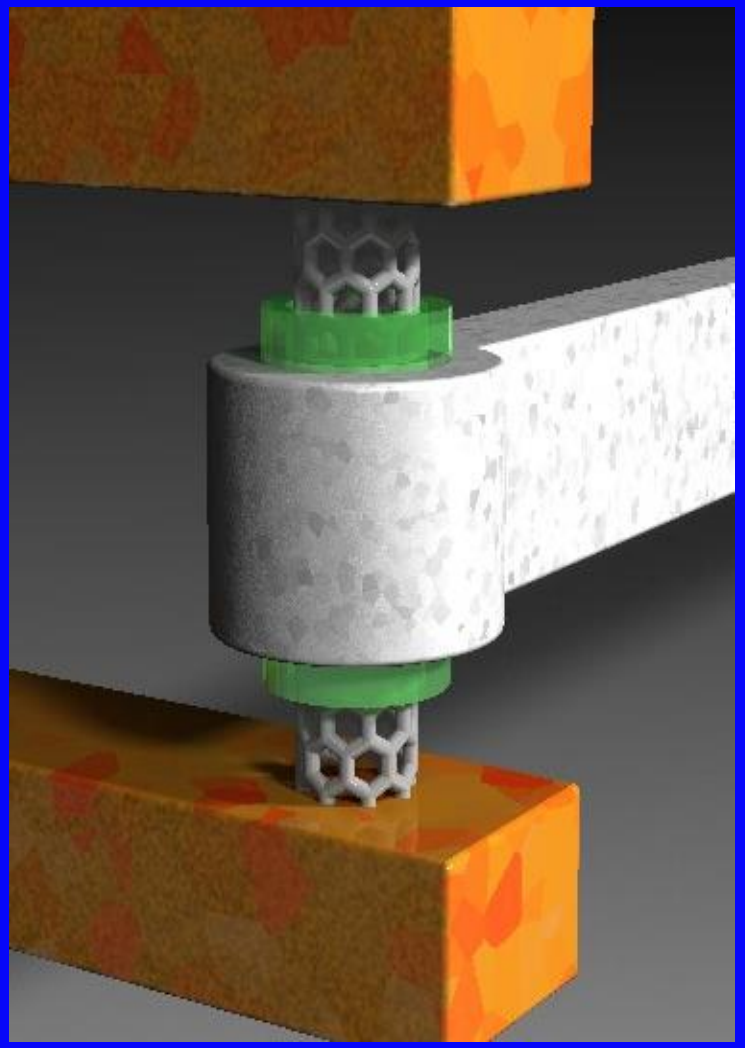
70 µA



20 µA

Source: Dick James, Chipworks, Gold Standard Simulations

Carbon Nanotube is still the best Semi material

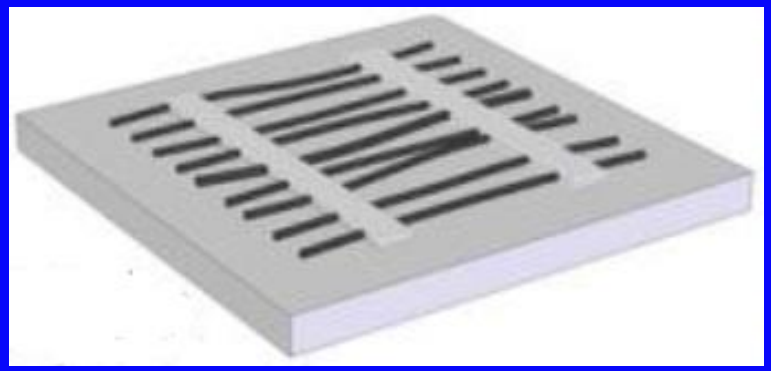


Kreupl, IFX 2003, US 7646045 B2

- Metallic S/D contacts: 7 kOhm *(Q. Cao et al., Science, 2015)*
- Gate–all-around demo‘ed (Franklin et al. , IEDM 2012)
- Dopant free (Kreupl SSDM 2005)
- High-k-compatible (Kreupl SSDM 2005)
- No dark-space effects (Knoch, EDL, 2008, Skotnicki & Boeuf, VLSI 2010)
- Scalability demo‘ed 9 nm (Franklin, NL. 2012, Kreupl, Nature 2012)
- Very small short channel effects (Franklin, Nano L. 2012)
- saturation @ low V and 9 nm (not in graphene or 2D) (Franklin, Nano L. 2012)
- 10x more energy efficient than Si technology (Shulaker, Springer. 2016)

Great News – how to proceed?

- Please give instructions
  - ➔ how to place billions of nanotubes with
    - one type of chirality
    - equal length
    - on a substrate
    - well aligned at some nanometer pitch
    - with a throughput of 120 wafers per hour



- Solution: Just issue a purchase order for the new Applied Materials *Nano-Wonder™* machine

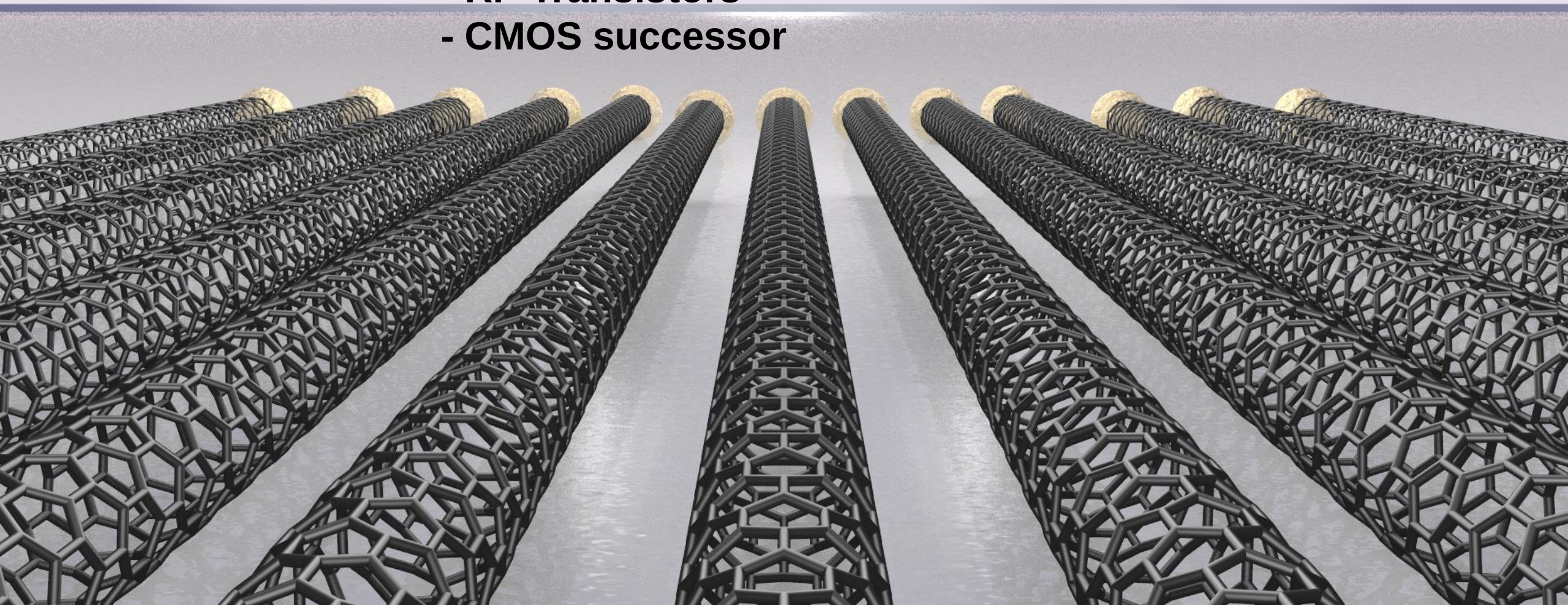
No - unfortunately – I am kidding

WireControl – a project sponsored by BMBF

Grow horizontally aligned CNTs on amorphous SiO2 on Si wafers

would enable:

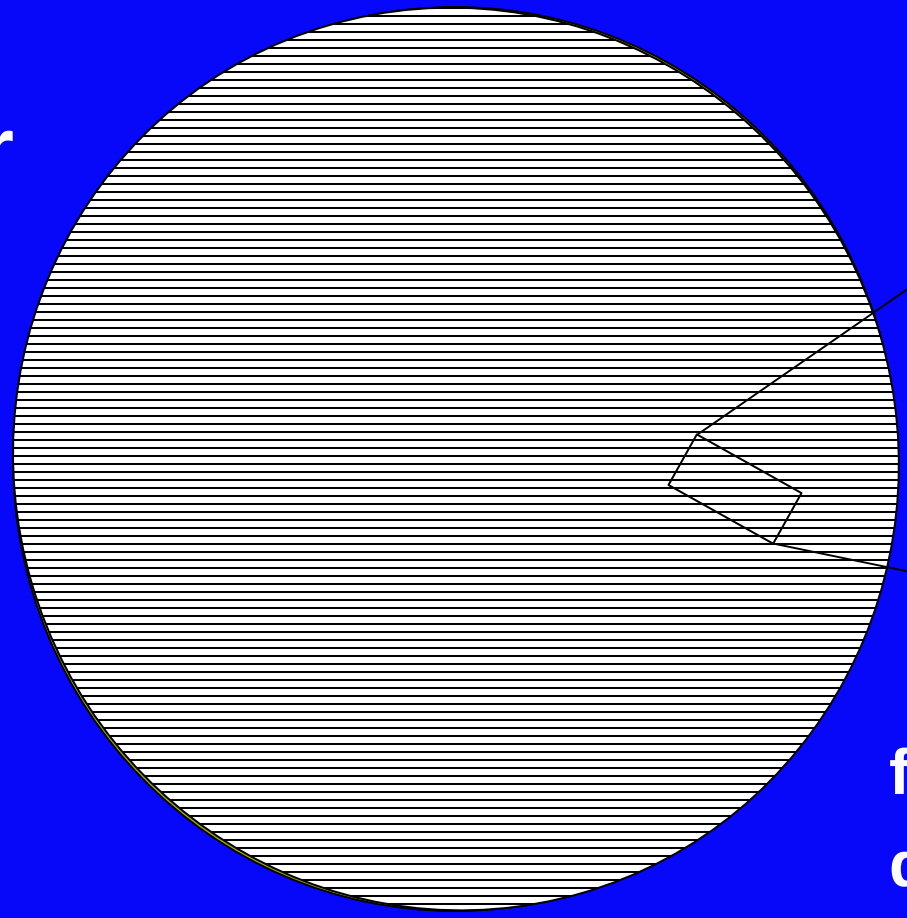
- **platform fo sensor application (do not need nm-scale)**
- **RF-Transistors**
- **CMOS successor**

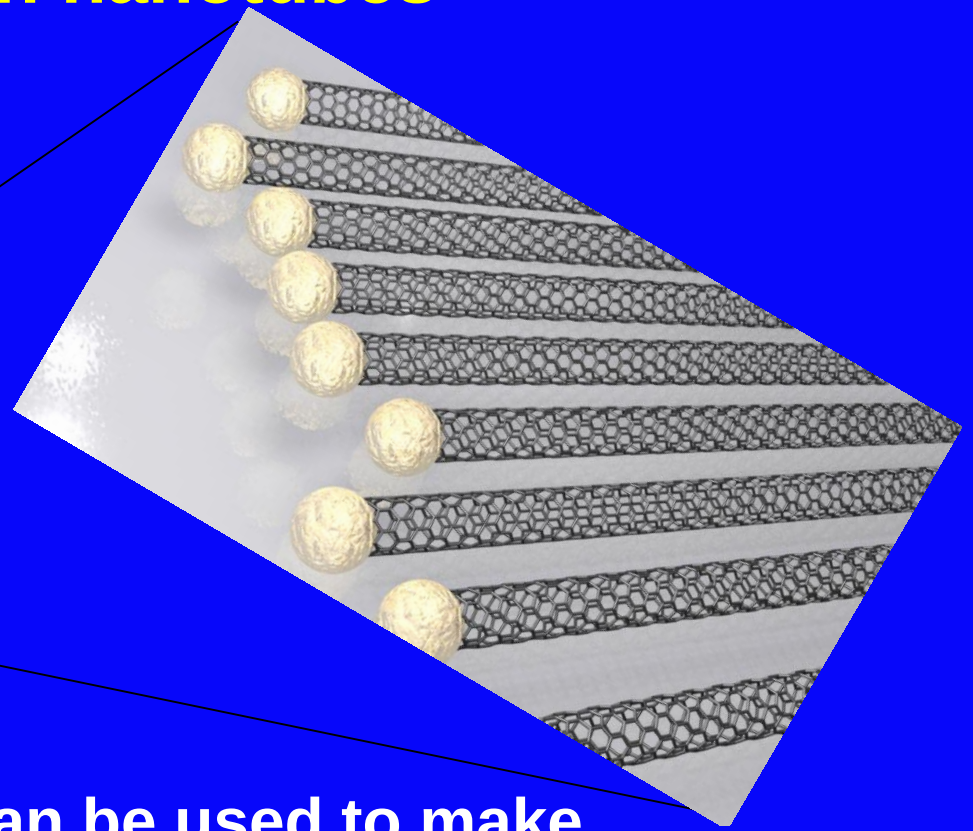


WireControl Goal

- Develop processes and methods to create substrates with **regularly aligned fabric of carbon nanotubes**

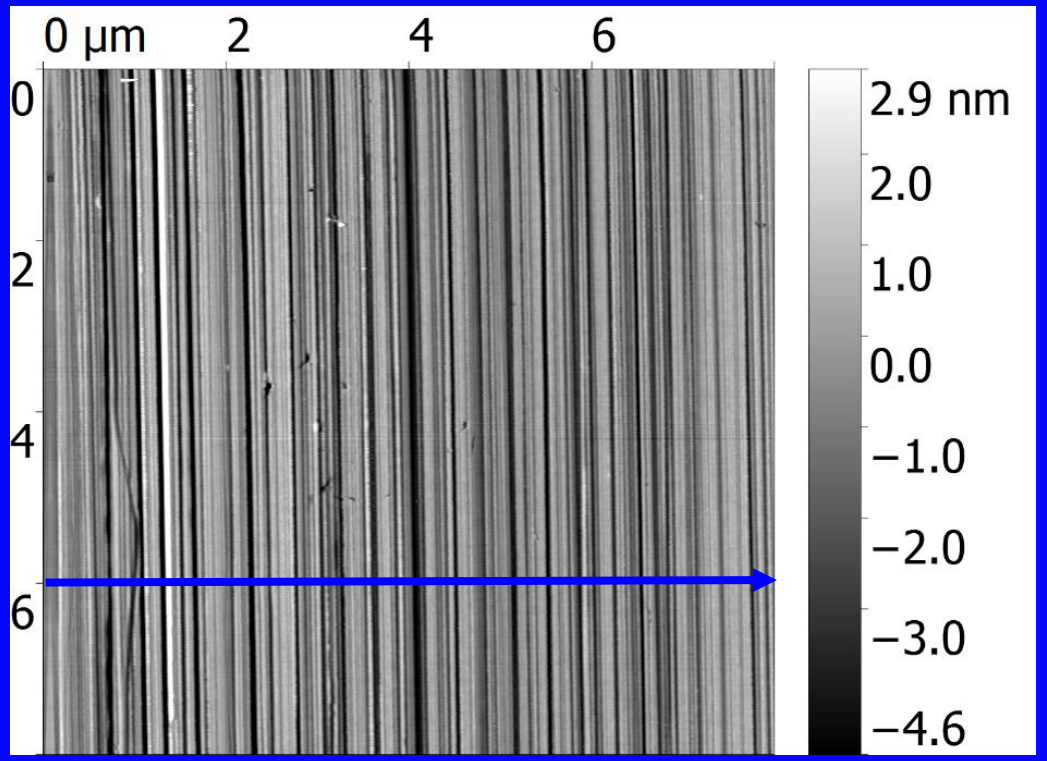
Wafer

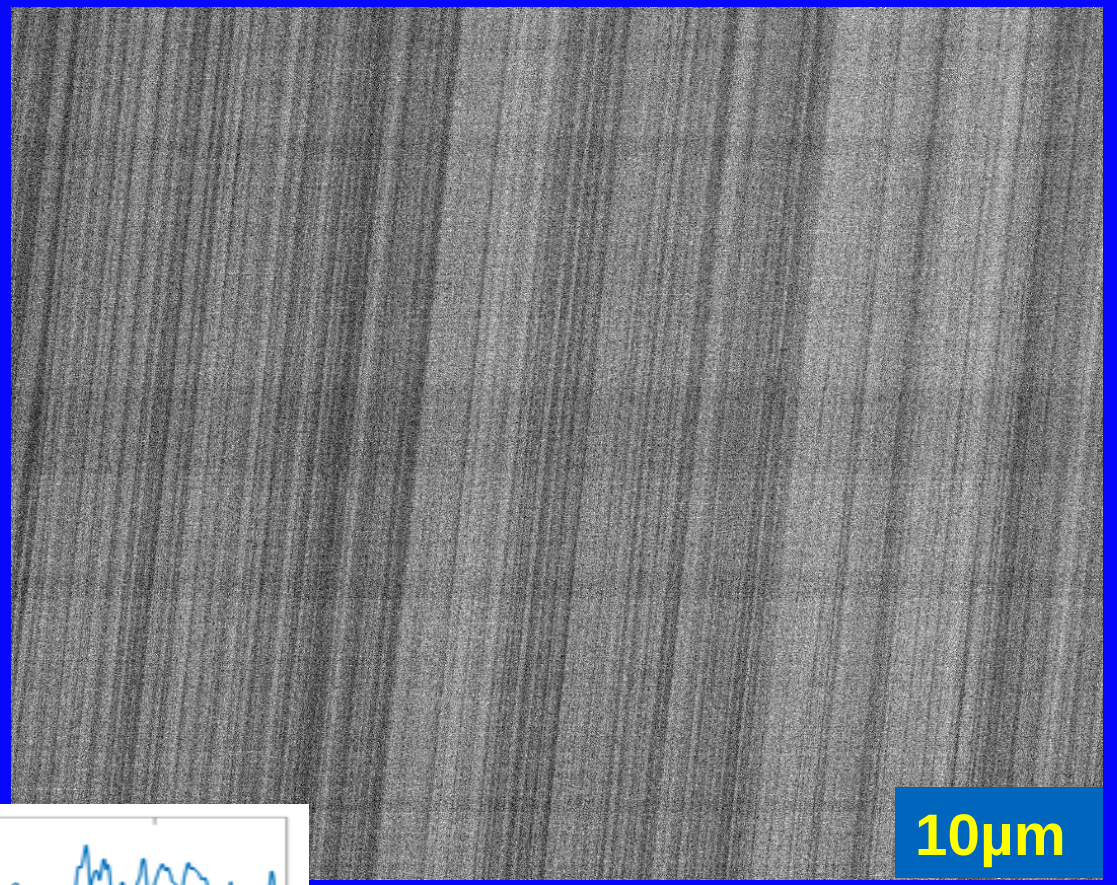


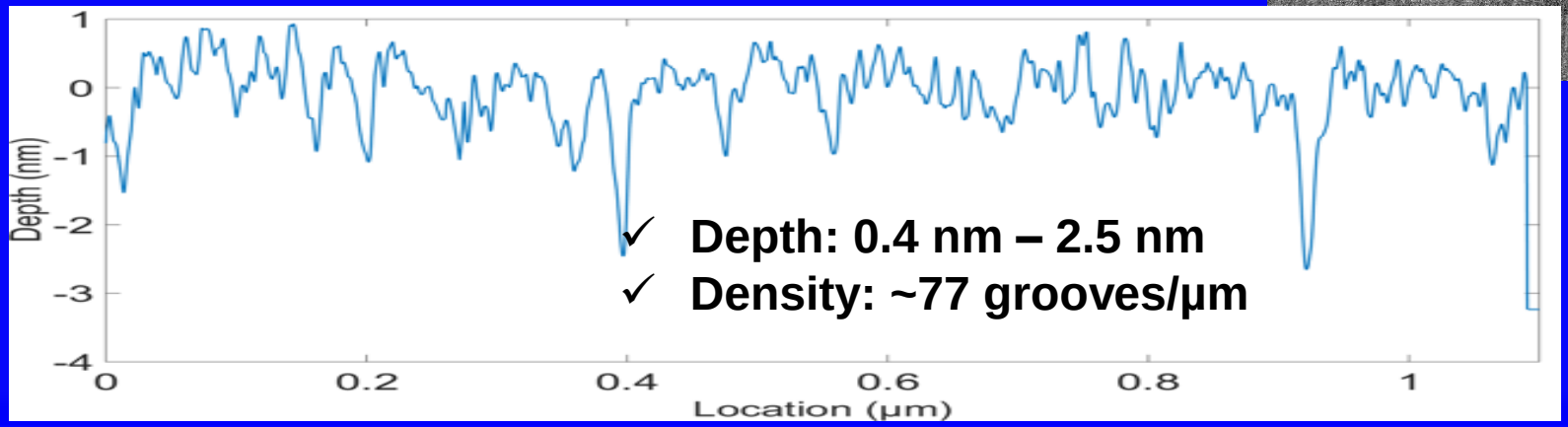


fabric can be used to make dies in conventional semiconductor fashion

First results: nm-sized grooves in amorphous SiO_2



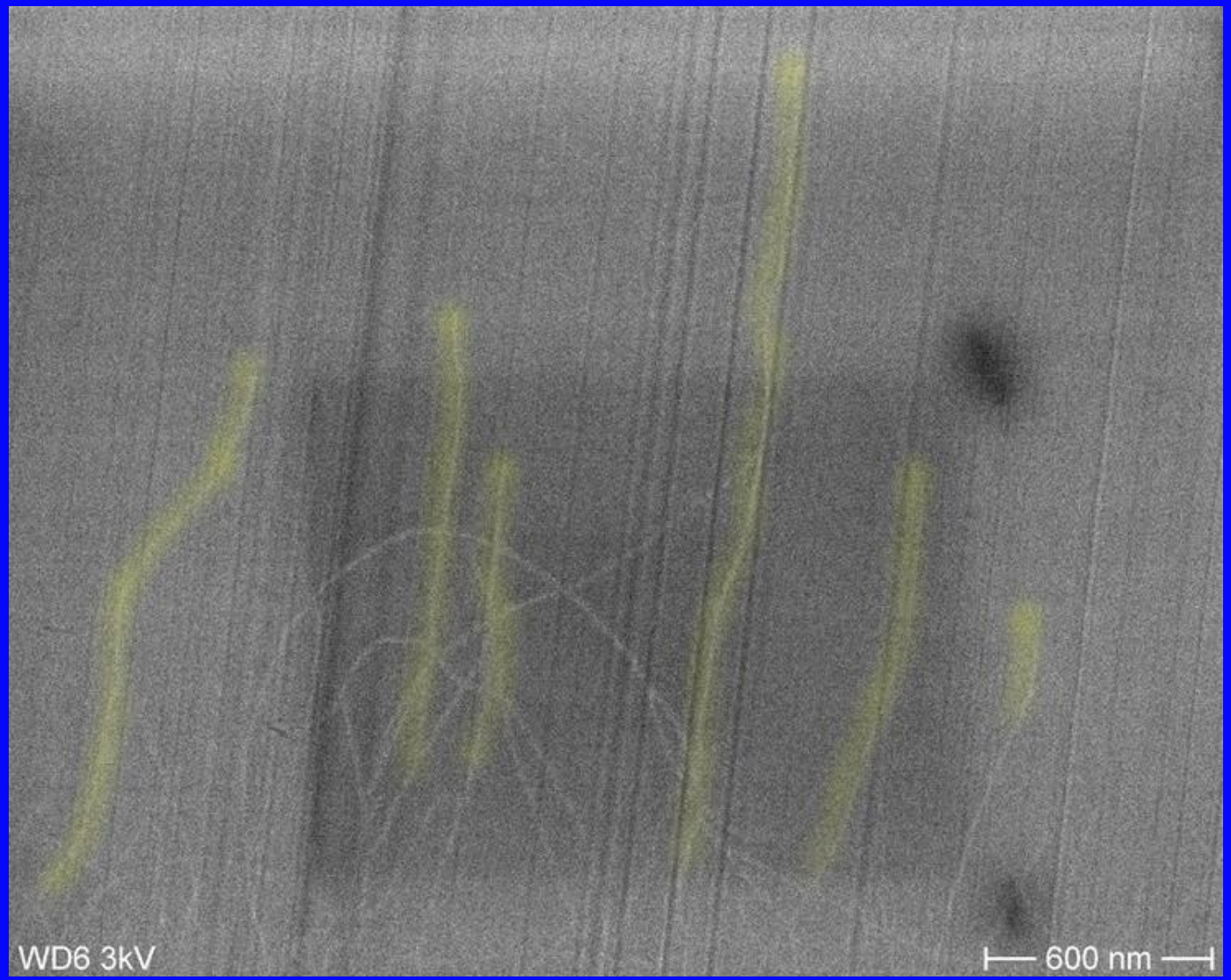




- ✓ **Depth: 0.4 nm – 2.5 nm**
- ✓ **Density: ~77 grooves/µm**

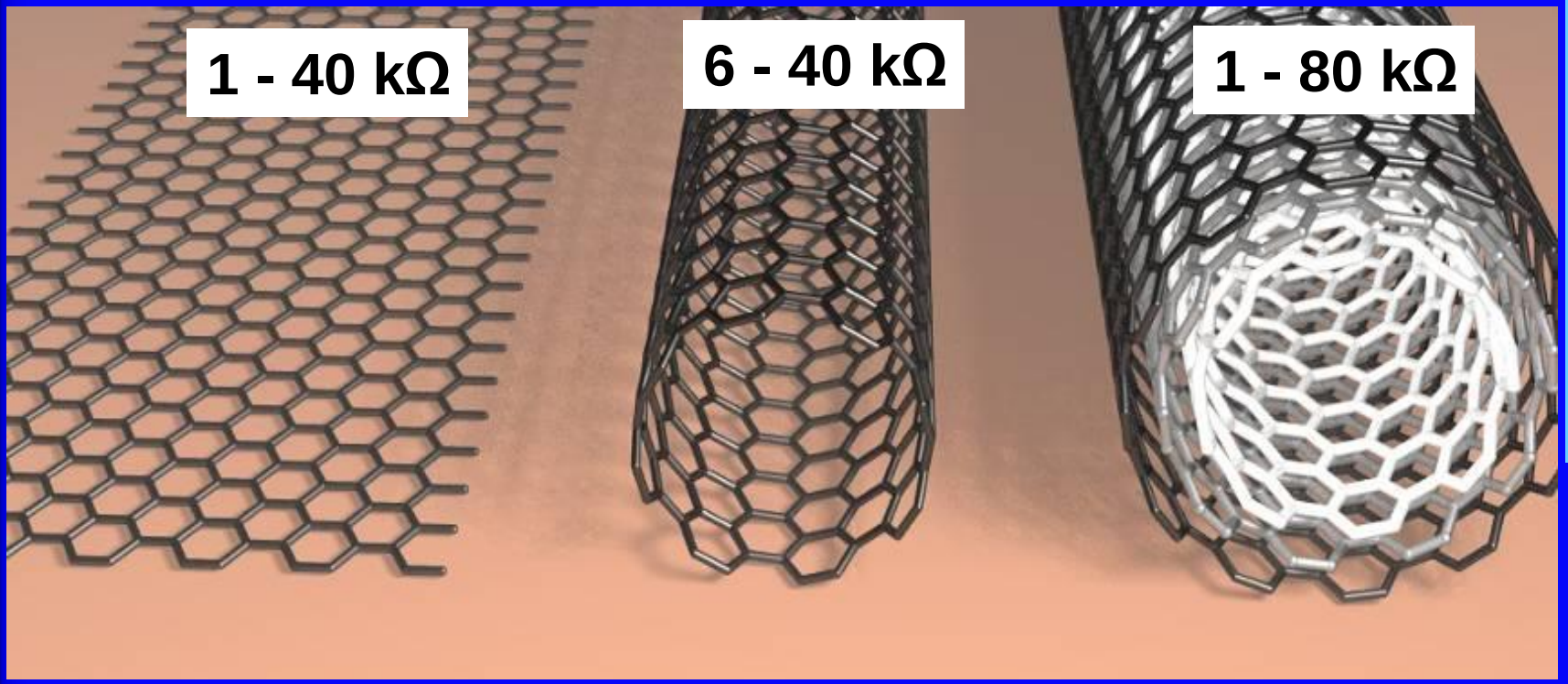
(HES, unpublished)

Nanotube growth along nano-grooves



(unpublished)

Carbon-based materials for interconnects

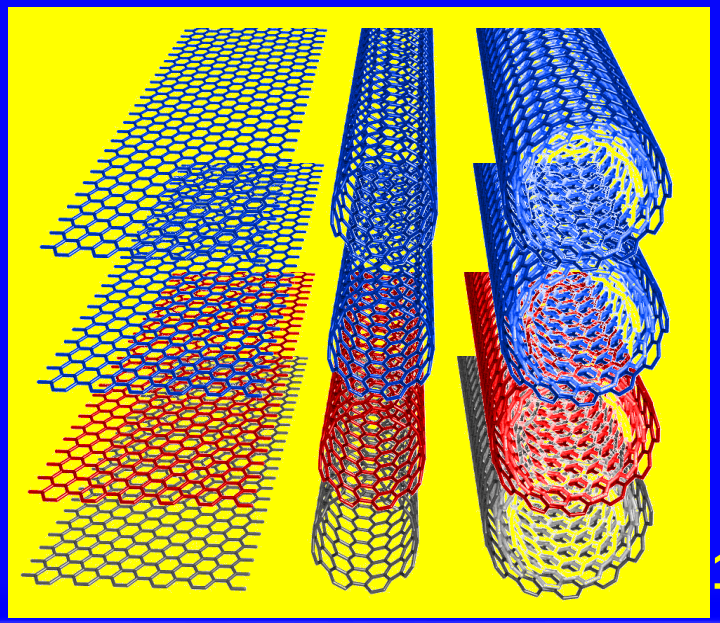


$$\frac{1}{R_\Sigma} = \sum_{i=1}^{n} \frac{1}{R_i}$$

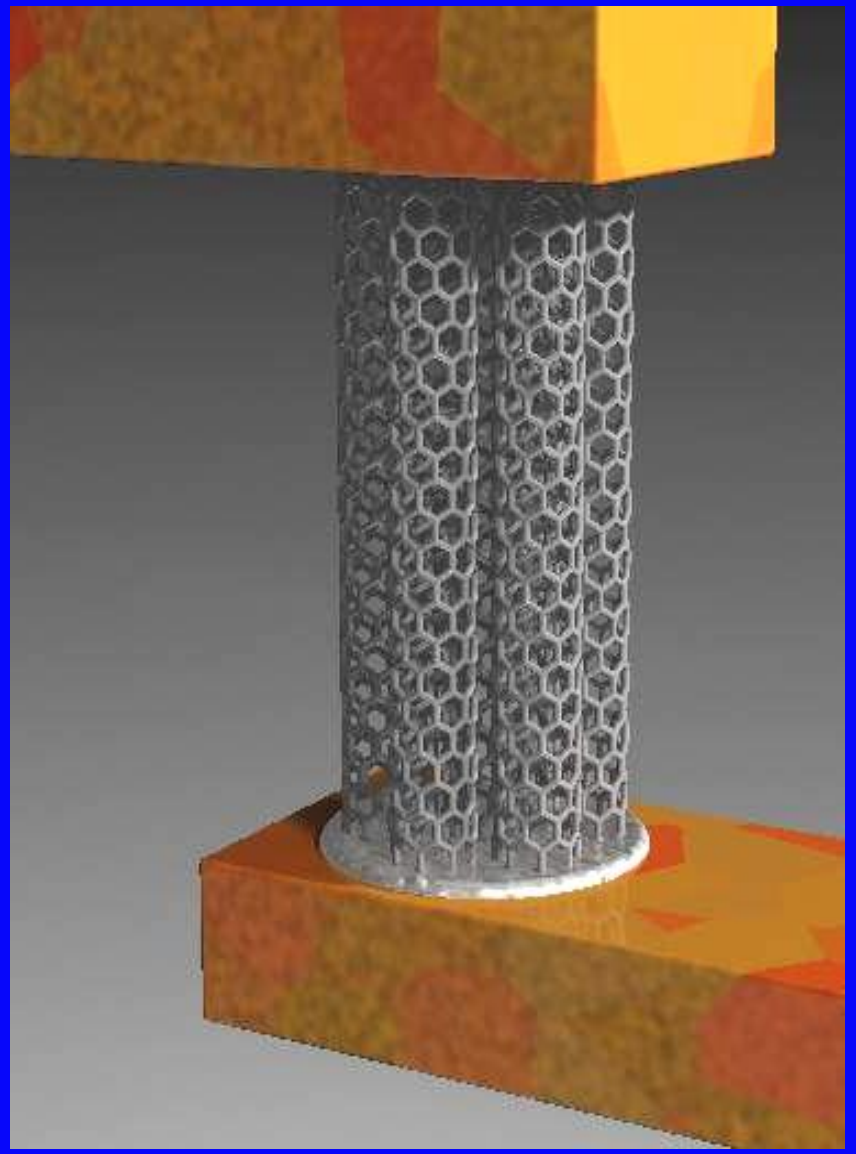
Graphene

Single-walled nanotube (SWCNT)

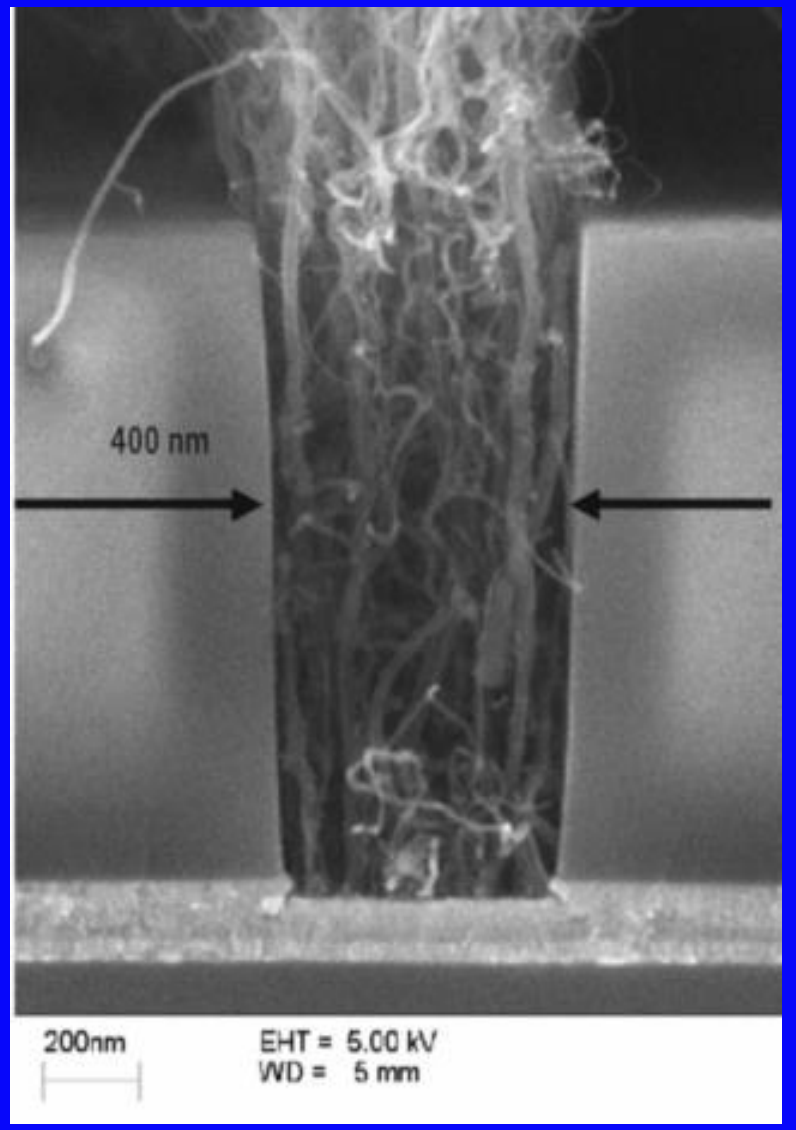
Multi-walled nanotube (MWCNT)



Nanotubes for vias and contact holes

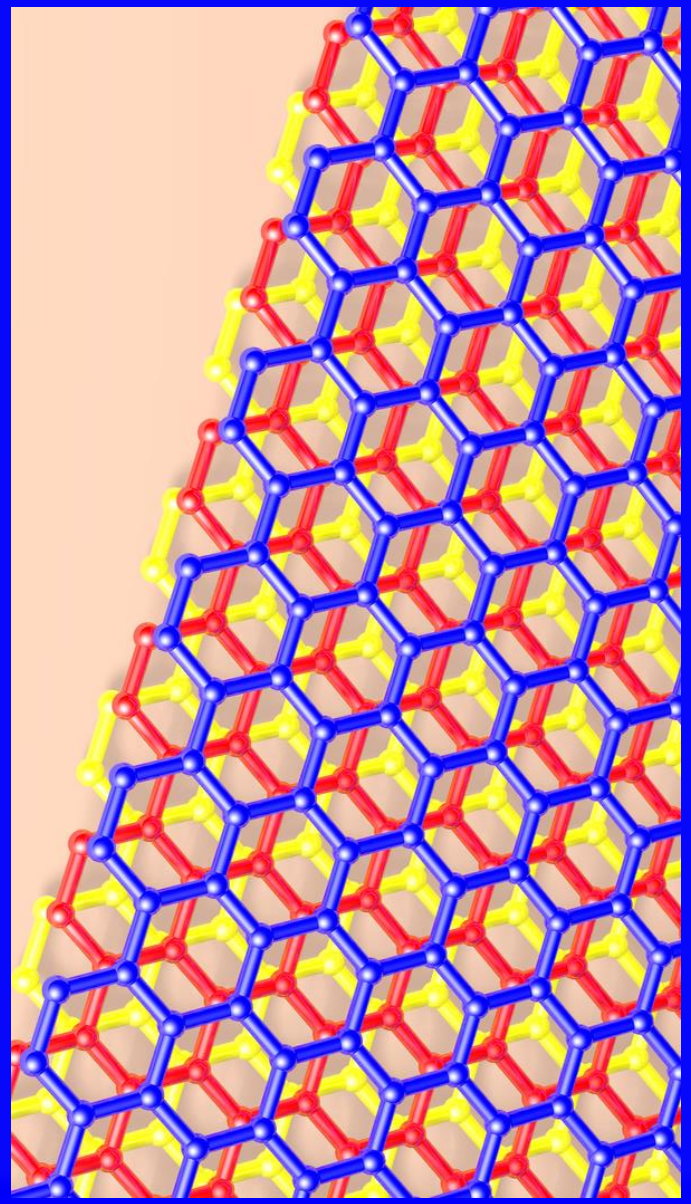


2000 - 2005

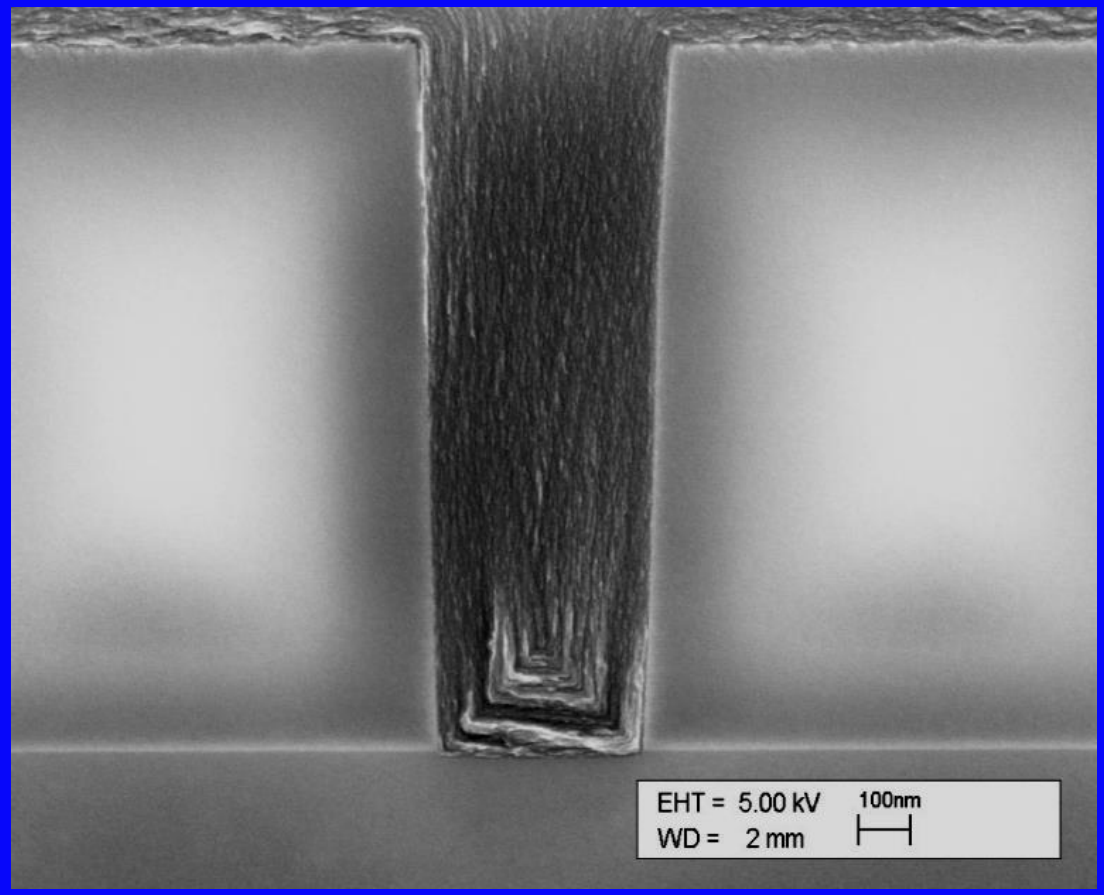


Kreupl et al., Microelectronic Engineering (2002), Kreupl et al., IEDM (2004)

Graphene multilayers for vias and contact holes

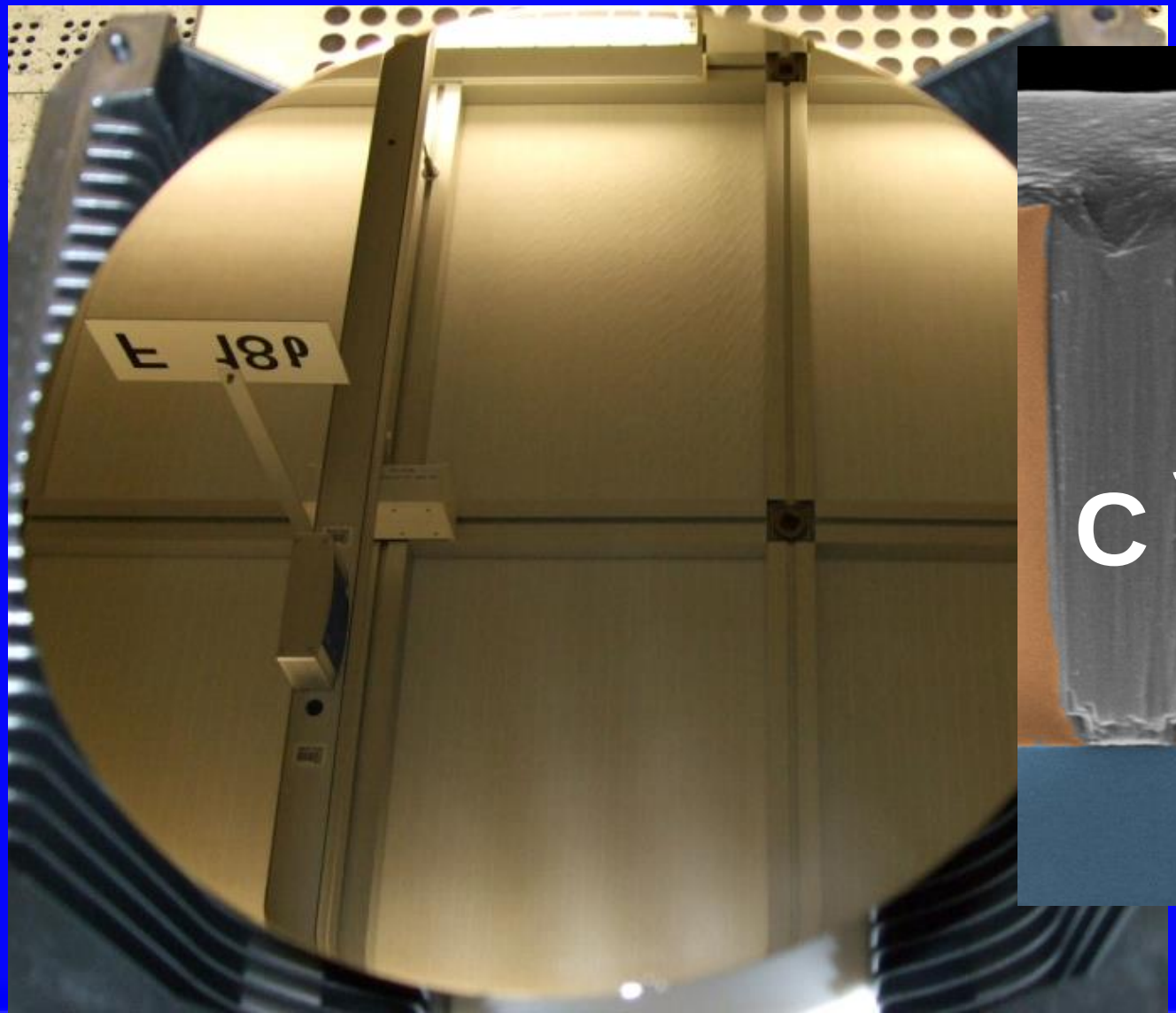


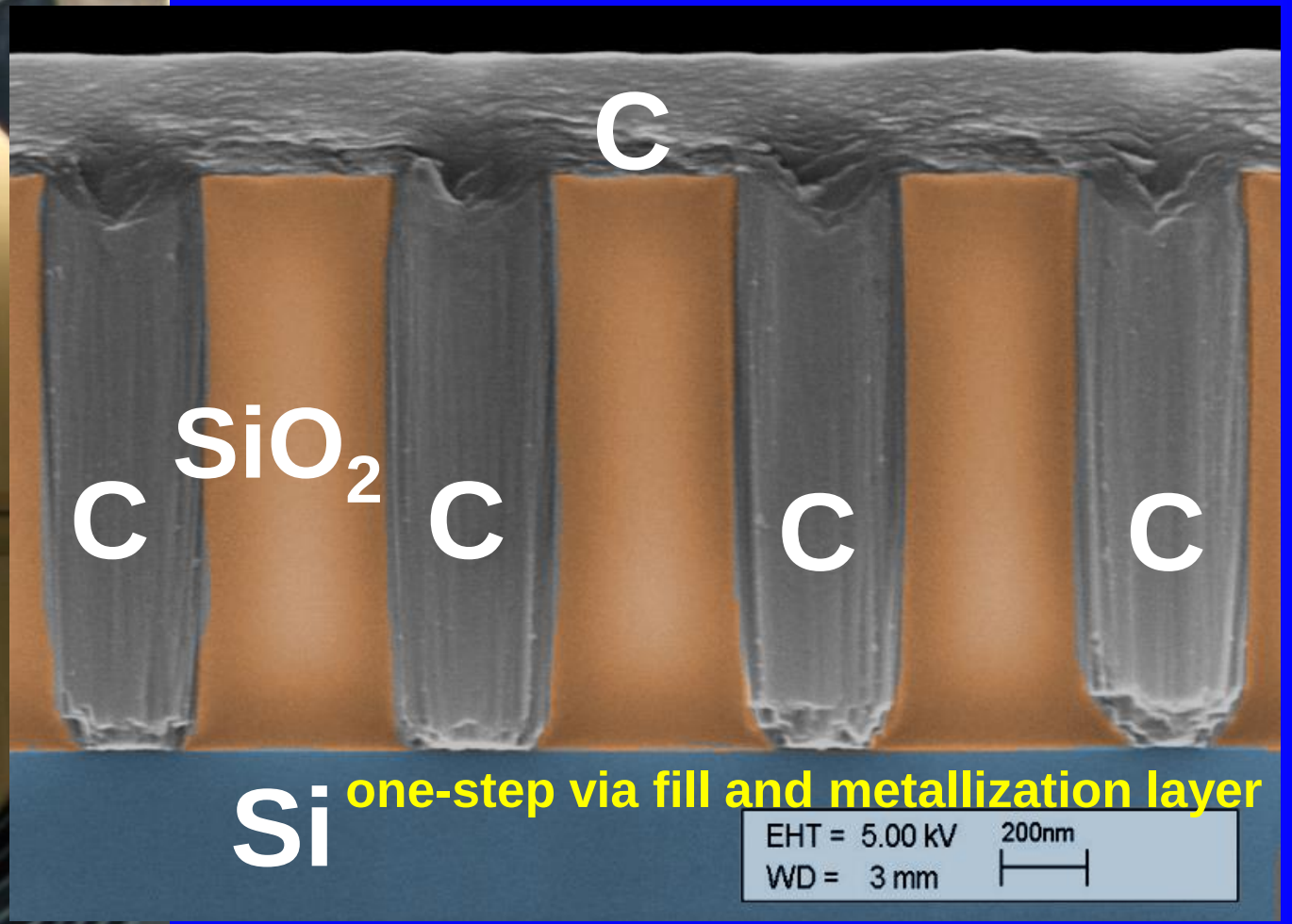
2003 – 202?



F. Kreupl, R. Seidel, W. Pamler, *Method of depositing a conductive material on a substrate and semiconductor contact device*, **patent DE10345393 (B4) (2003)**

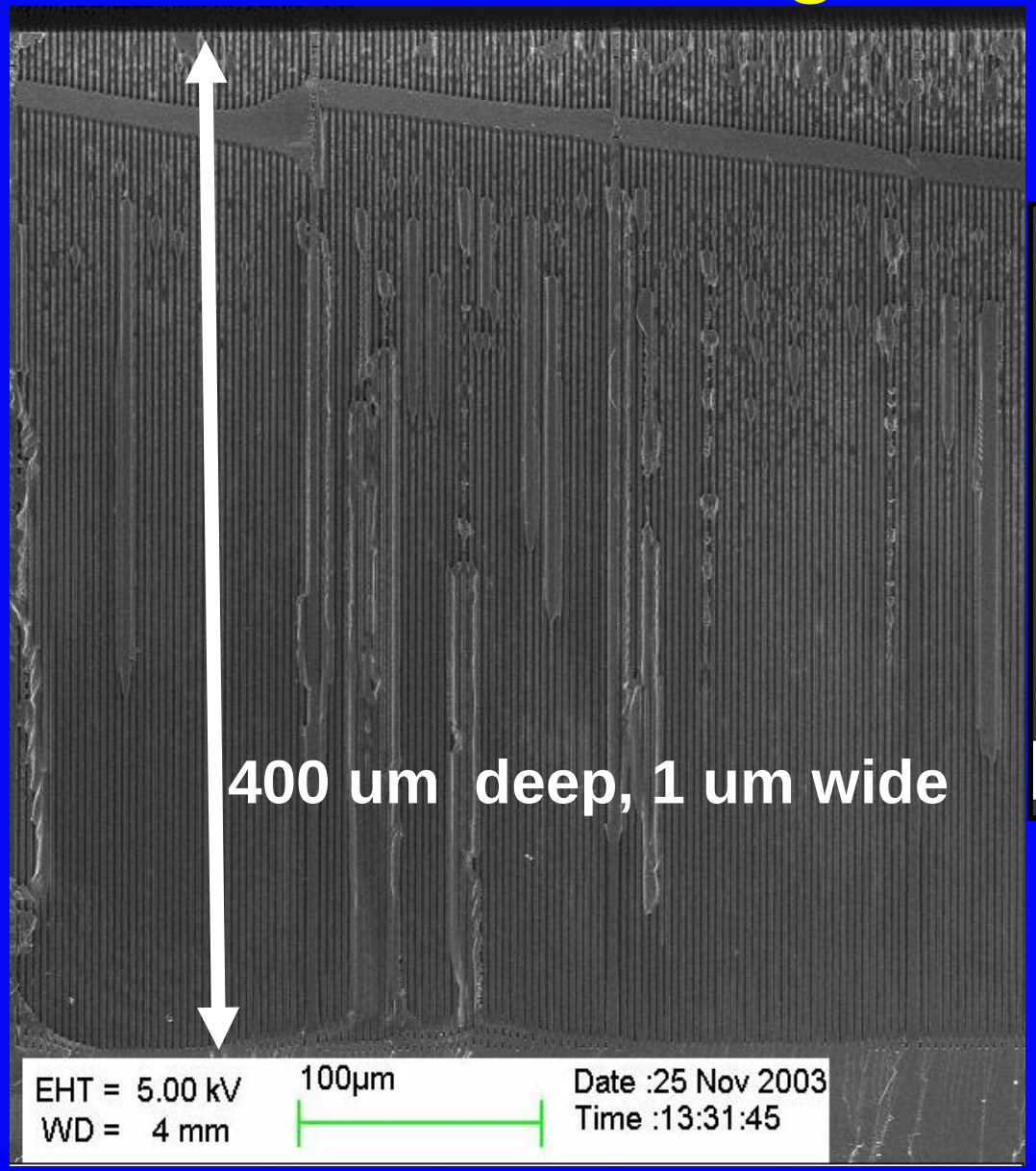
Highly conductive graphenic carbon on 8”wafer

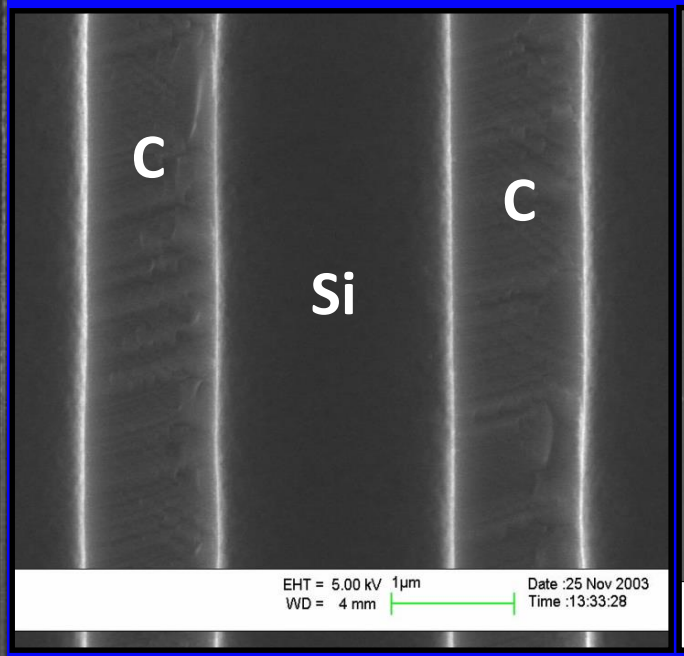


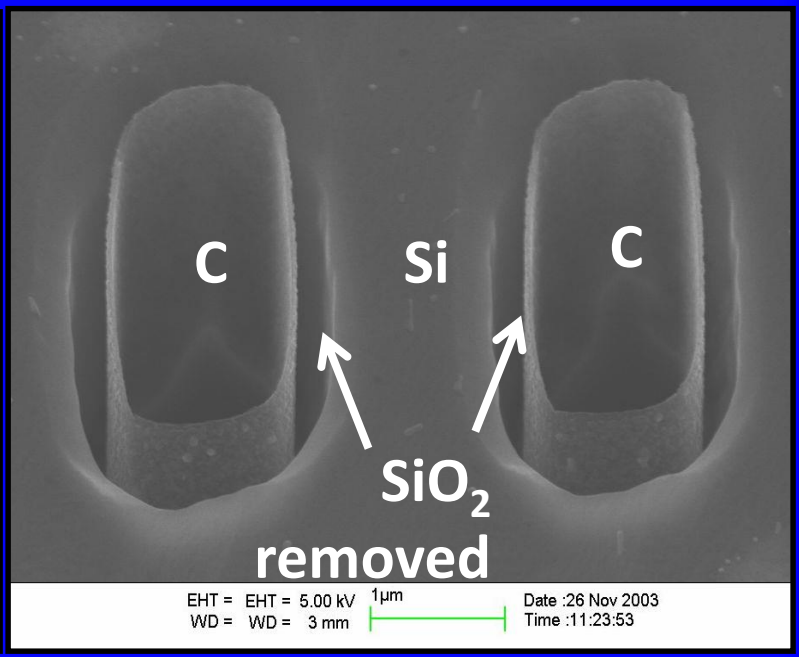


F. Kreupl, *MRS P*. 303, 1, (2011)

Through Silicon Via Fill



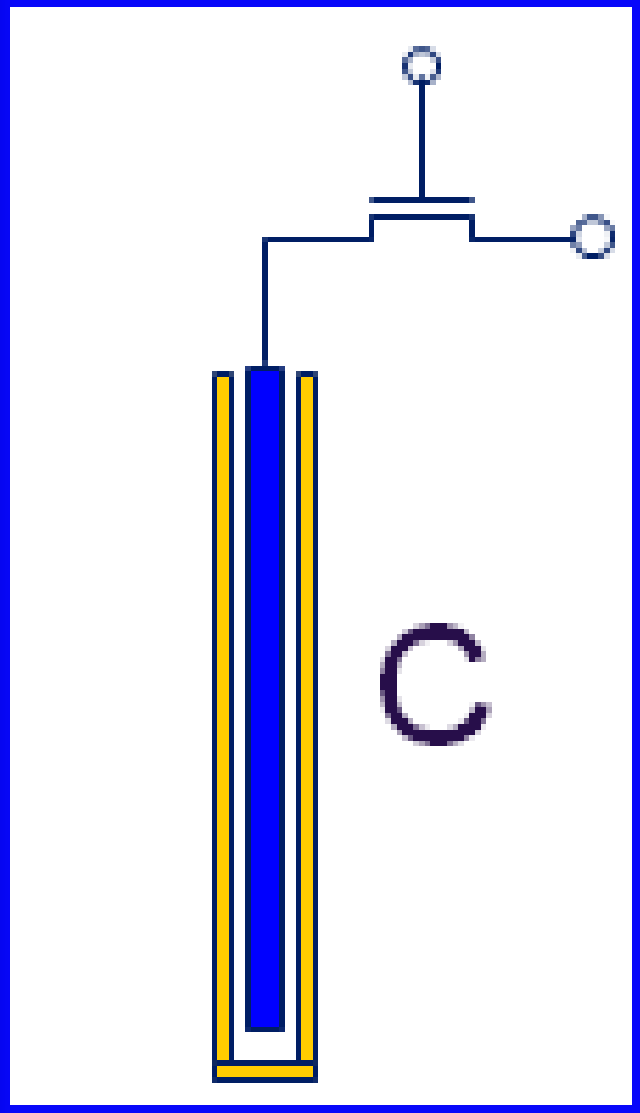


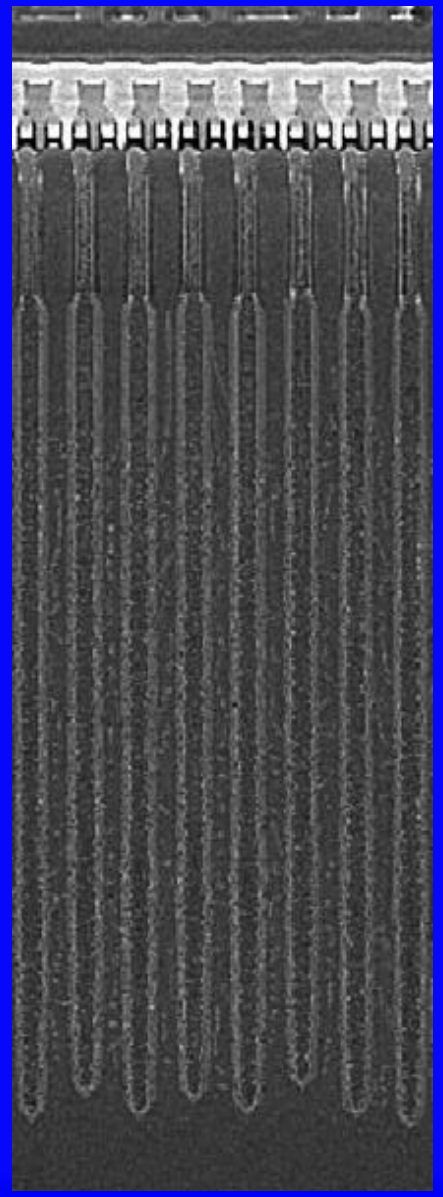


CVD-C fills aspect ratios > 400: Via-first approach possible

F. Kreupl, *MRS P*. 303, 1, (2011)

Application: Trench Fill for the DRAM Technology



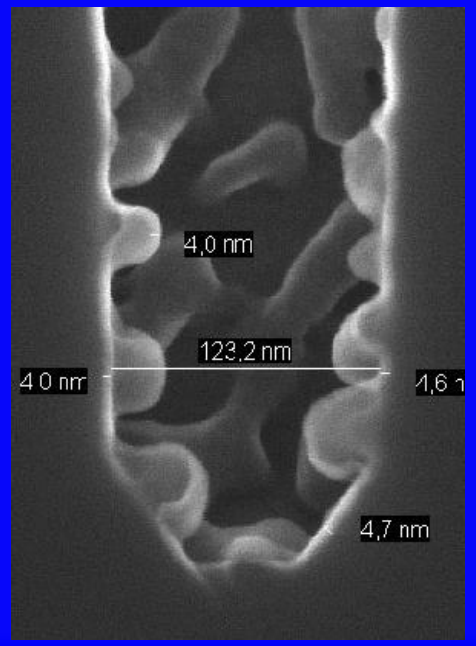


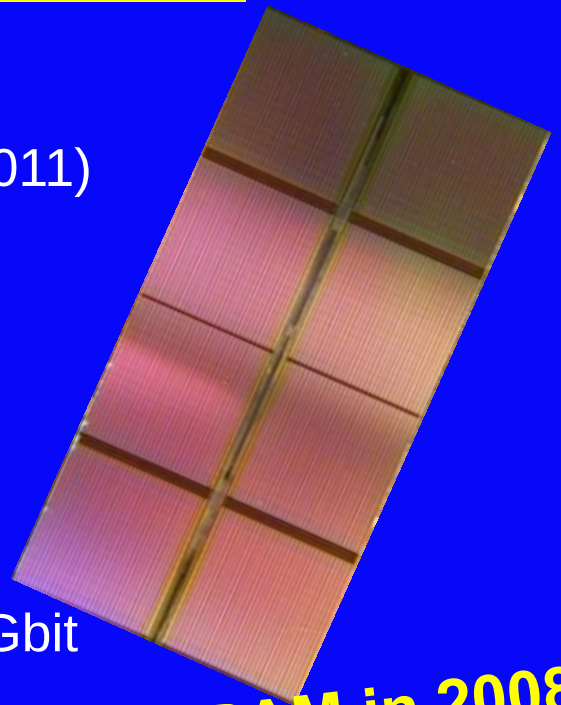
Aspect ratio of > 80:
extremely difficult to fill

Application in a 30 Bill. $ market

Aichmayr et al., VLSI 2007

F. Kreupl, *MRS P*. 303, 1, (2011)



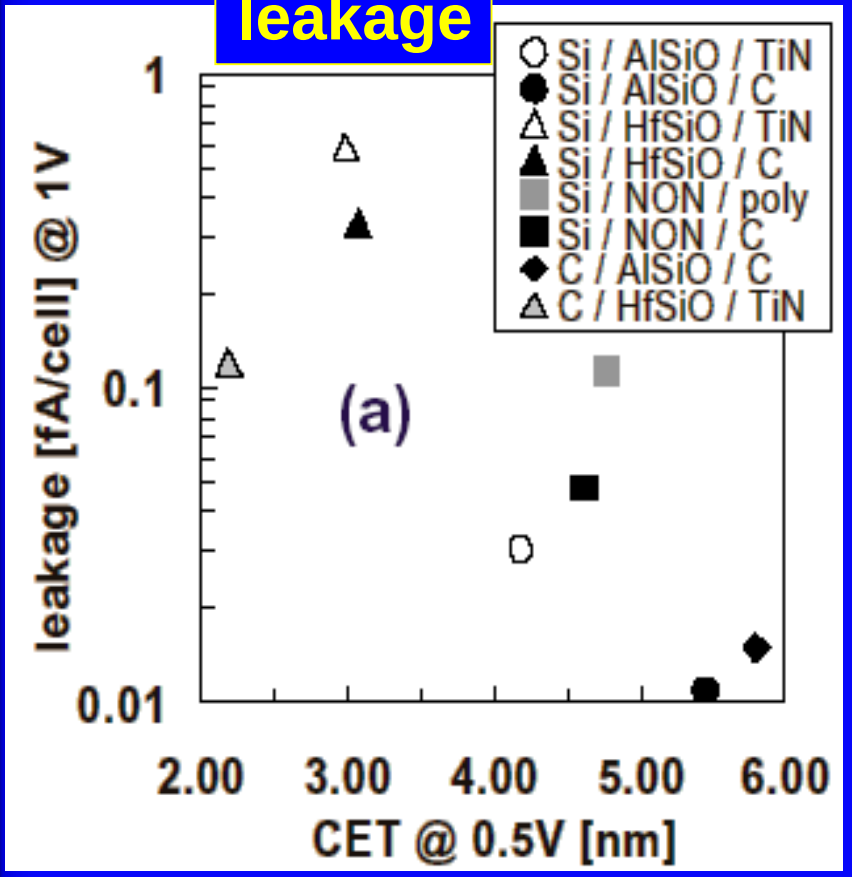


1Gbit

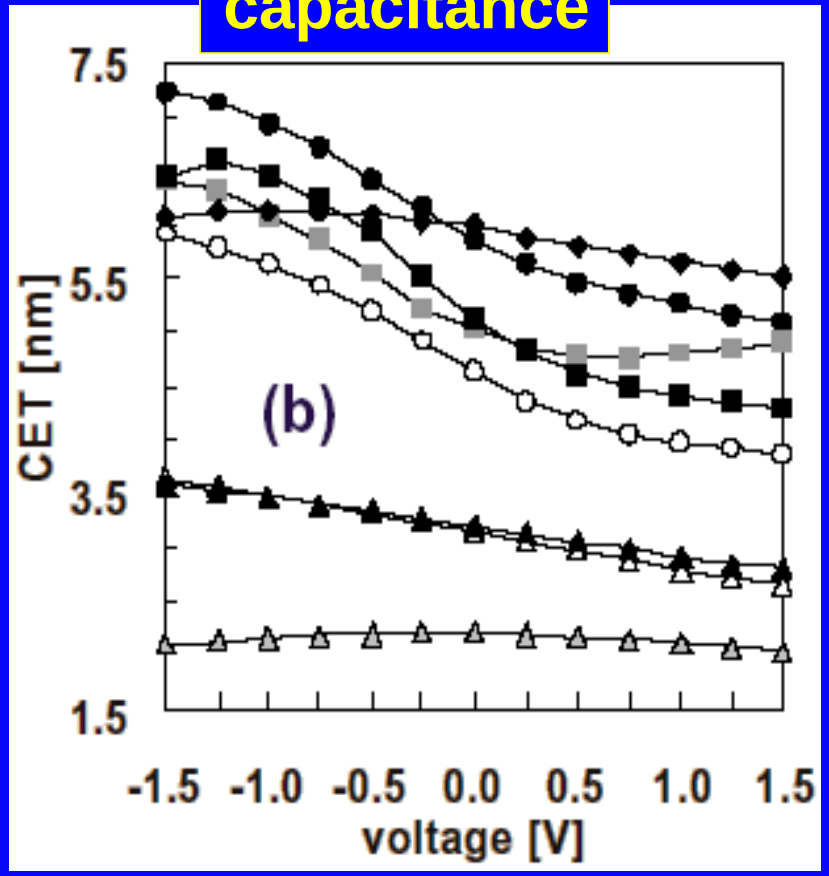
Qimonda DRAM in 2008 had "carbon inside"

Carbon / high-k Trench Capacitor

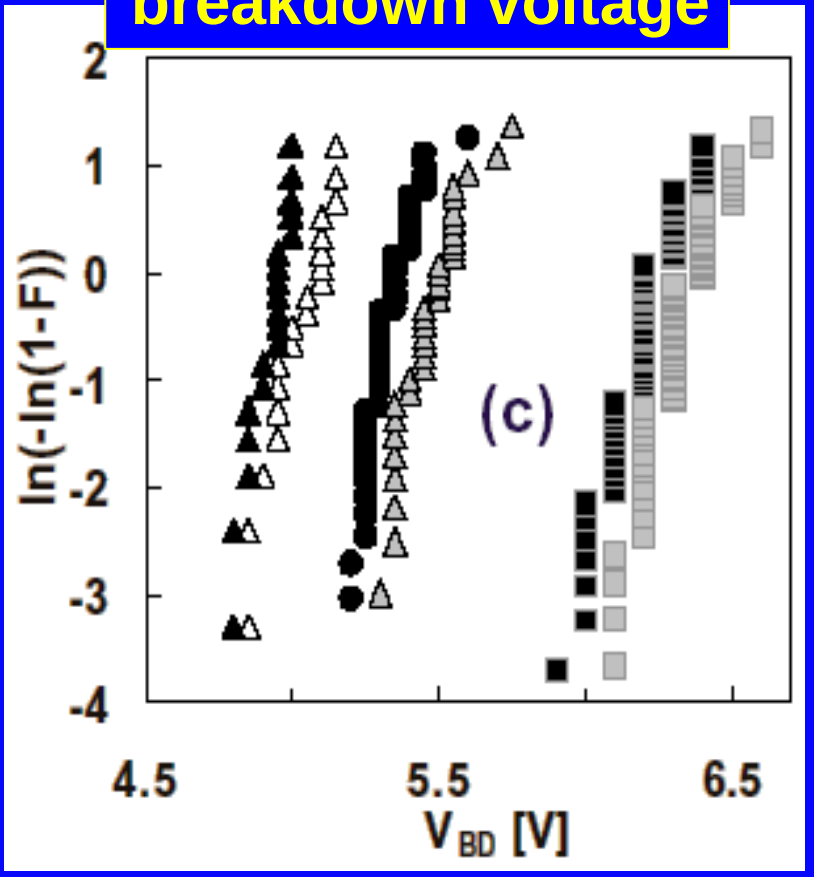
leakage



capacitance



breakdown voltage



- **compatibility** with a range of **high-k materials** shown
- cost and complexity effective **alternative metal electrode**,
- match **leakage, reliability and speed** requirements

Aichmayr et al., VLSI 2007
Boeschke et al. IEEE EDL , 2009

Metal-Semiconductor Contacts

source drain contacts, contacts to a pn-diode

Signal Detection

High Speed Switching

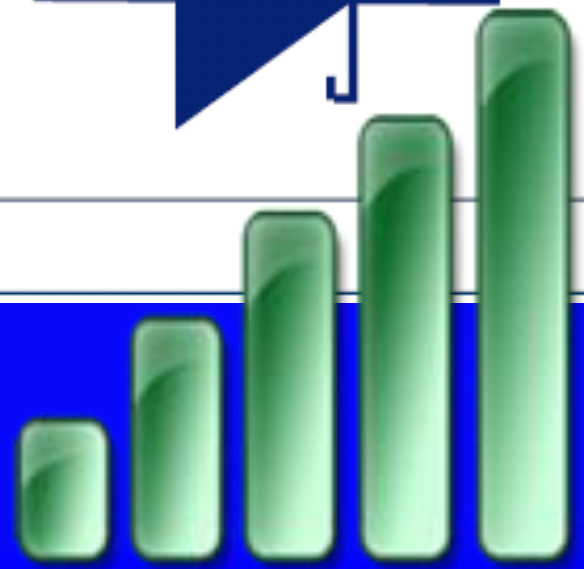
Mixer Application

Schottky Diodes

Circuit Protection

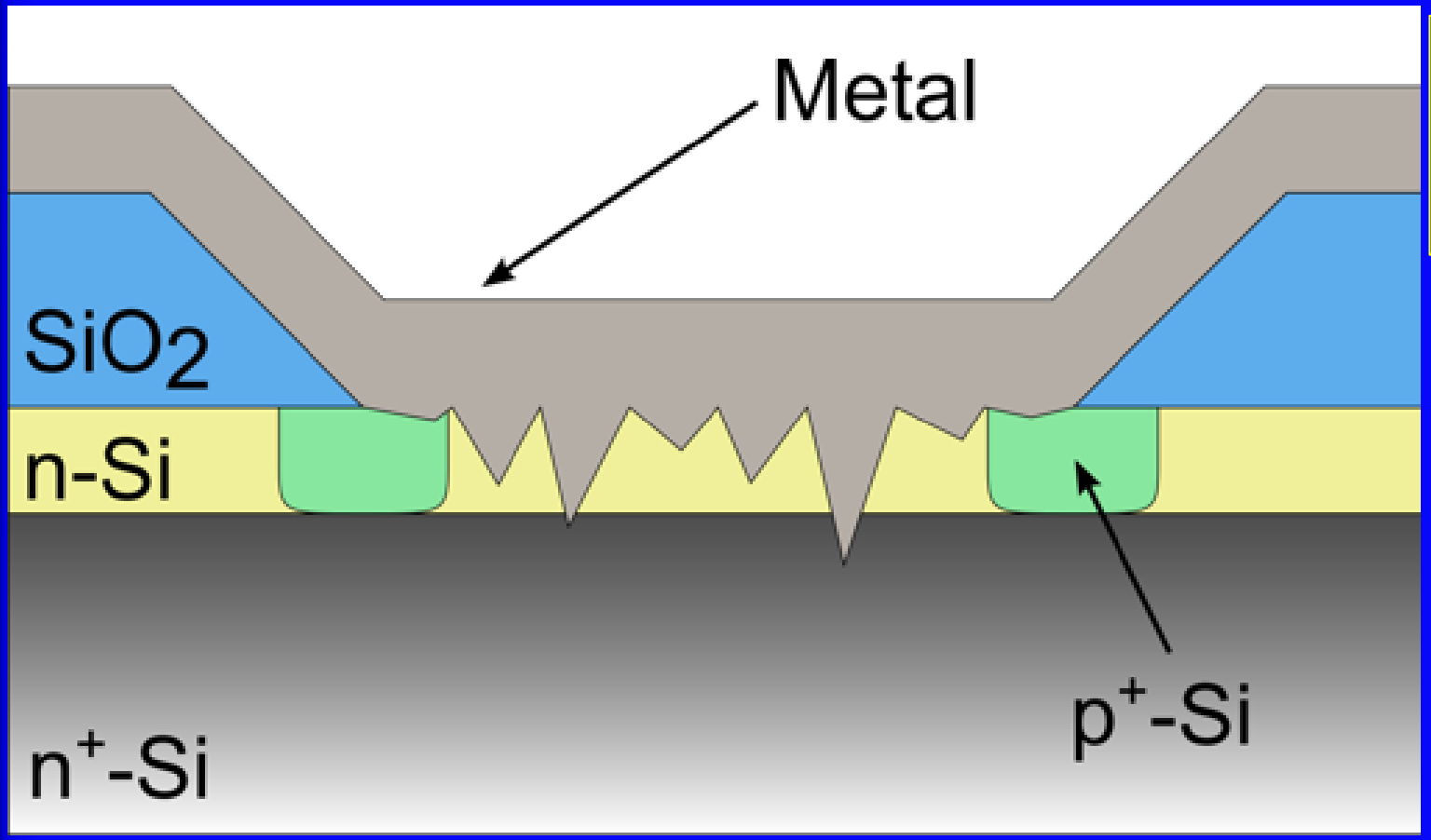
Clamping

Rectifying



F. Kreupl, *MRS P*. 303, 1, (2011)

ESD damage in metal-Si contacts

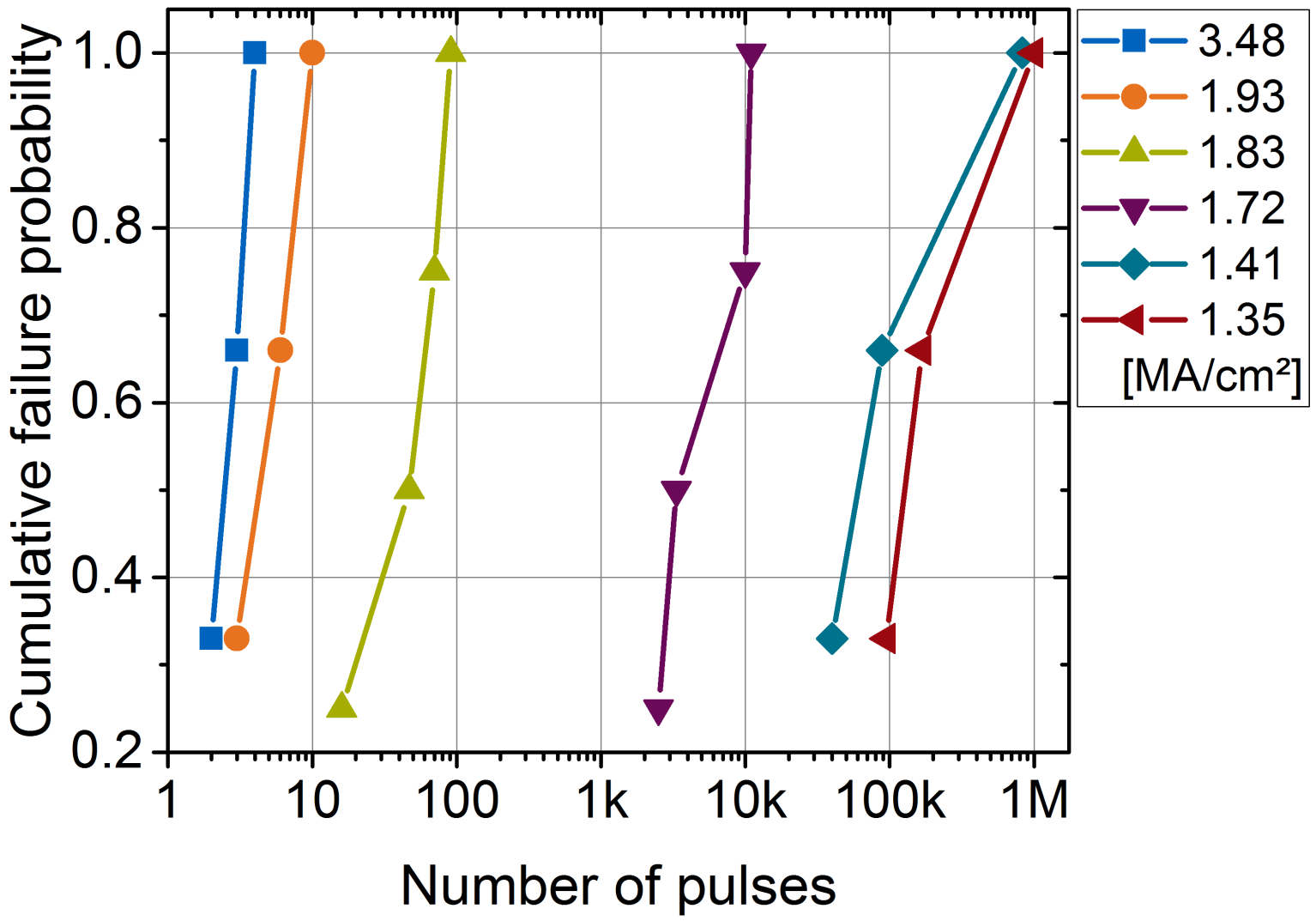


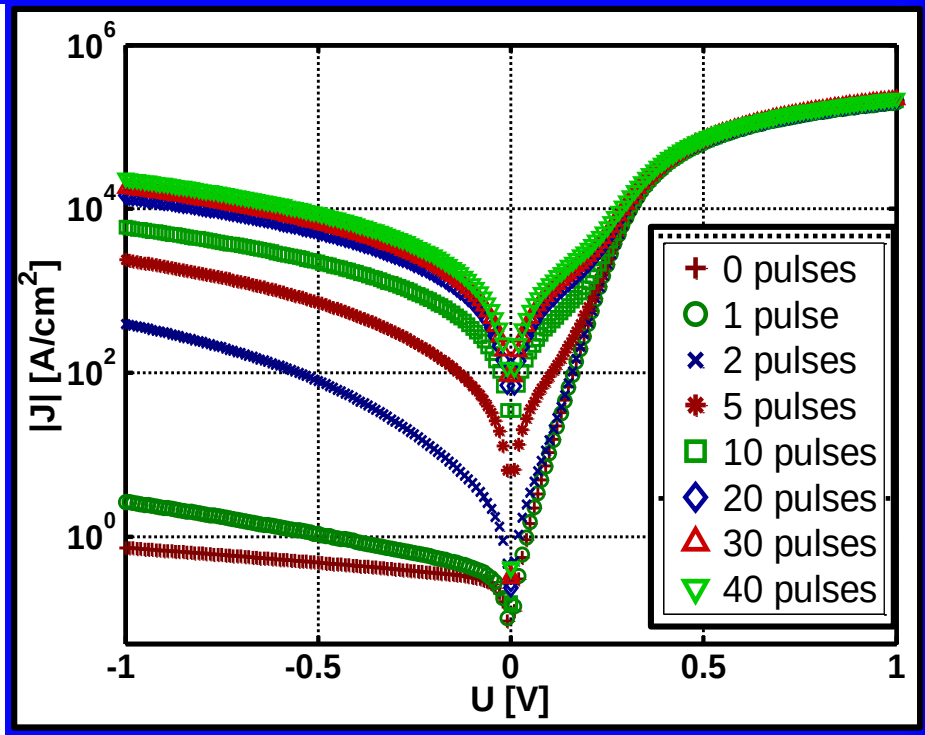
$$\frac{TdS}{Vdt} = \frac{P}{V} = jE = j^2\rho$$

P: power
T: temperature
V: volume
dS/dt: entropy prod. rate
j: current density
E: electrical field
ρ: electrical resistivity

typical Electro-Static Discharge (ESD) pulse ~ 100ns

ESD damage in Infineon BAT 15 TiSi-Si-diodes

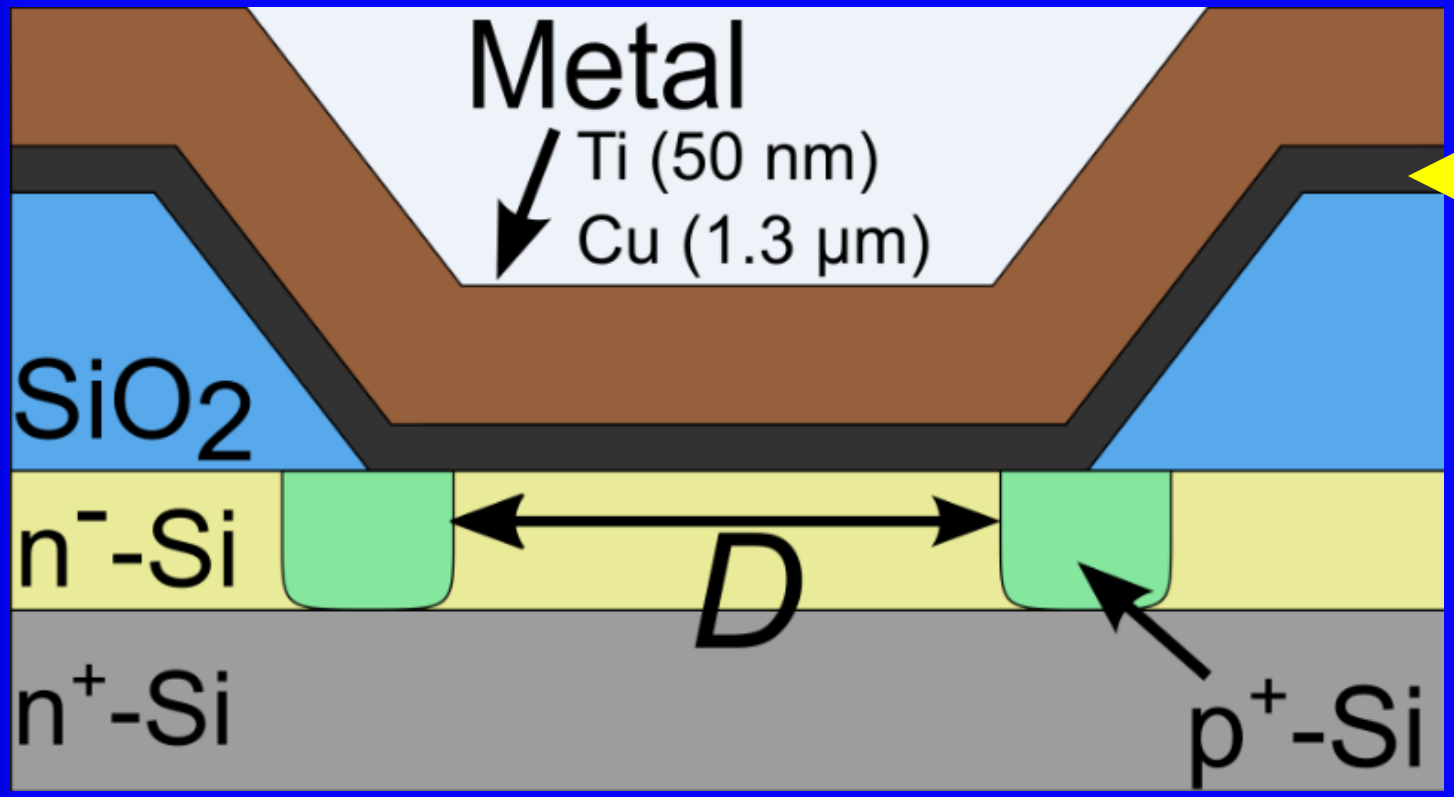




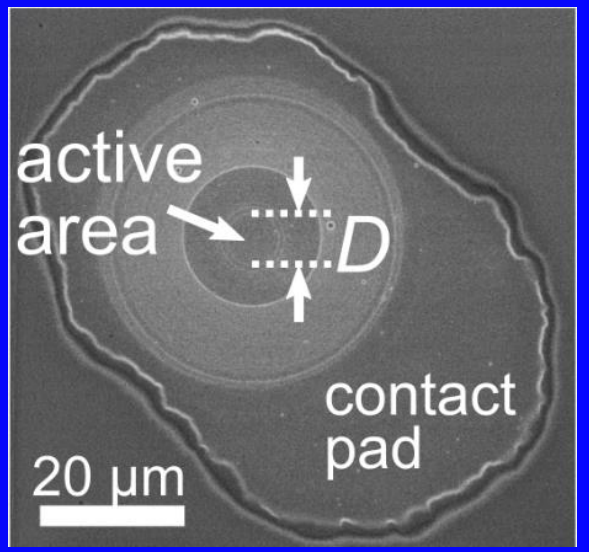
Infineon BAT15 dead after 2 pulses @ 3.5 MA/cm²

(Max Stelzer et al., submitted

Comparison: TiSi-based BAT 15 versus C-Si

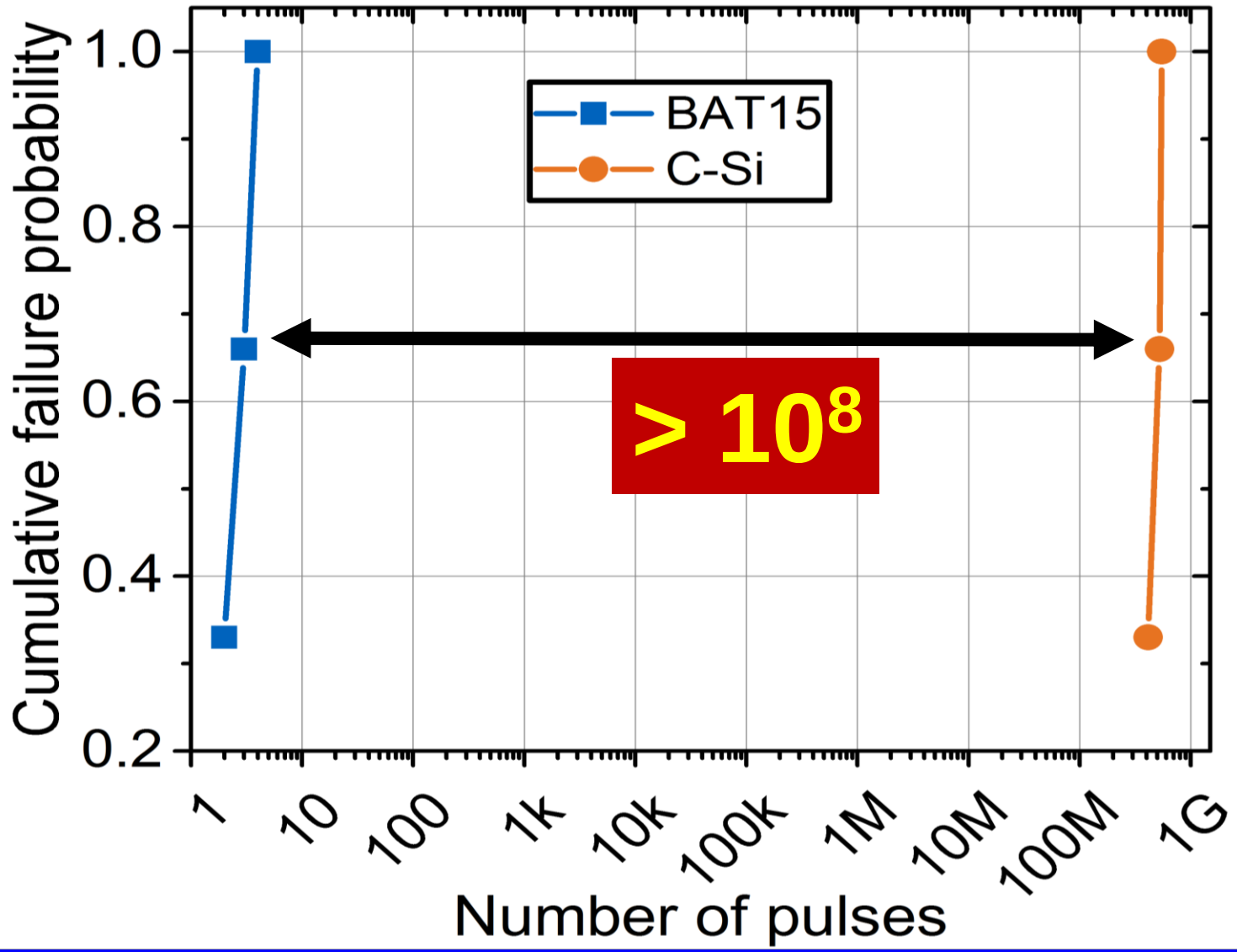


TiSi or C



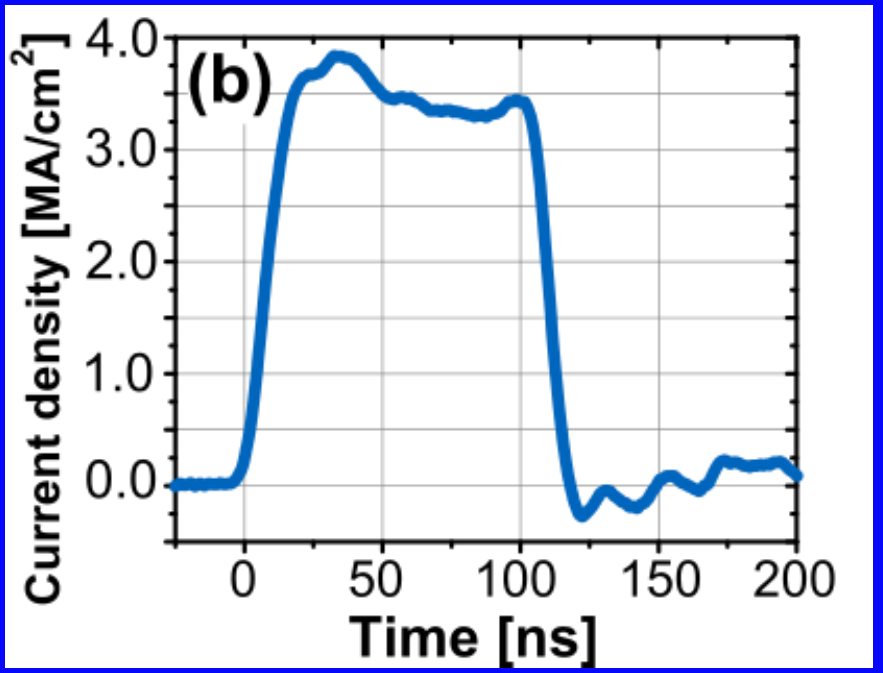
- Both diodes were fabricated on the same Si vehicle (dopants etc)
- ~150 nm n- Si is very sensible to trace amounts of contamination

ESD improvement by carbon-Si contact



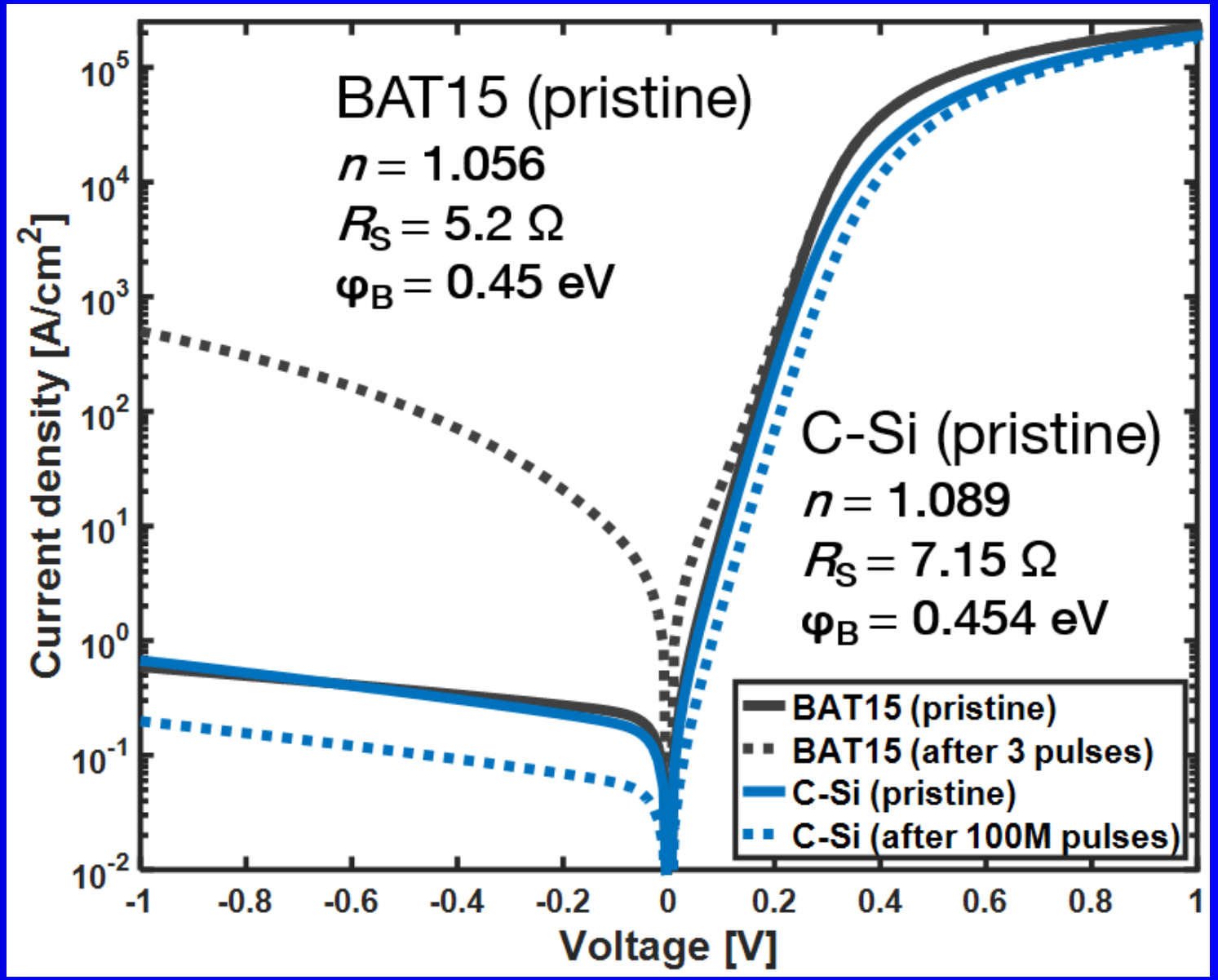
Tested with
100 ns pulses @ 3.5 MA/cm²

> 10^8 improvement



(Max Stelzer et al., submitted)

Comparison: TiSi-Si versus C-Si



TiSi & C-Si same I(V)

TiSi & C-Si same low barrier (0.45 eV)

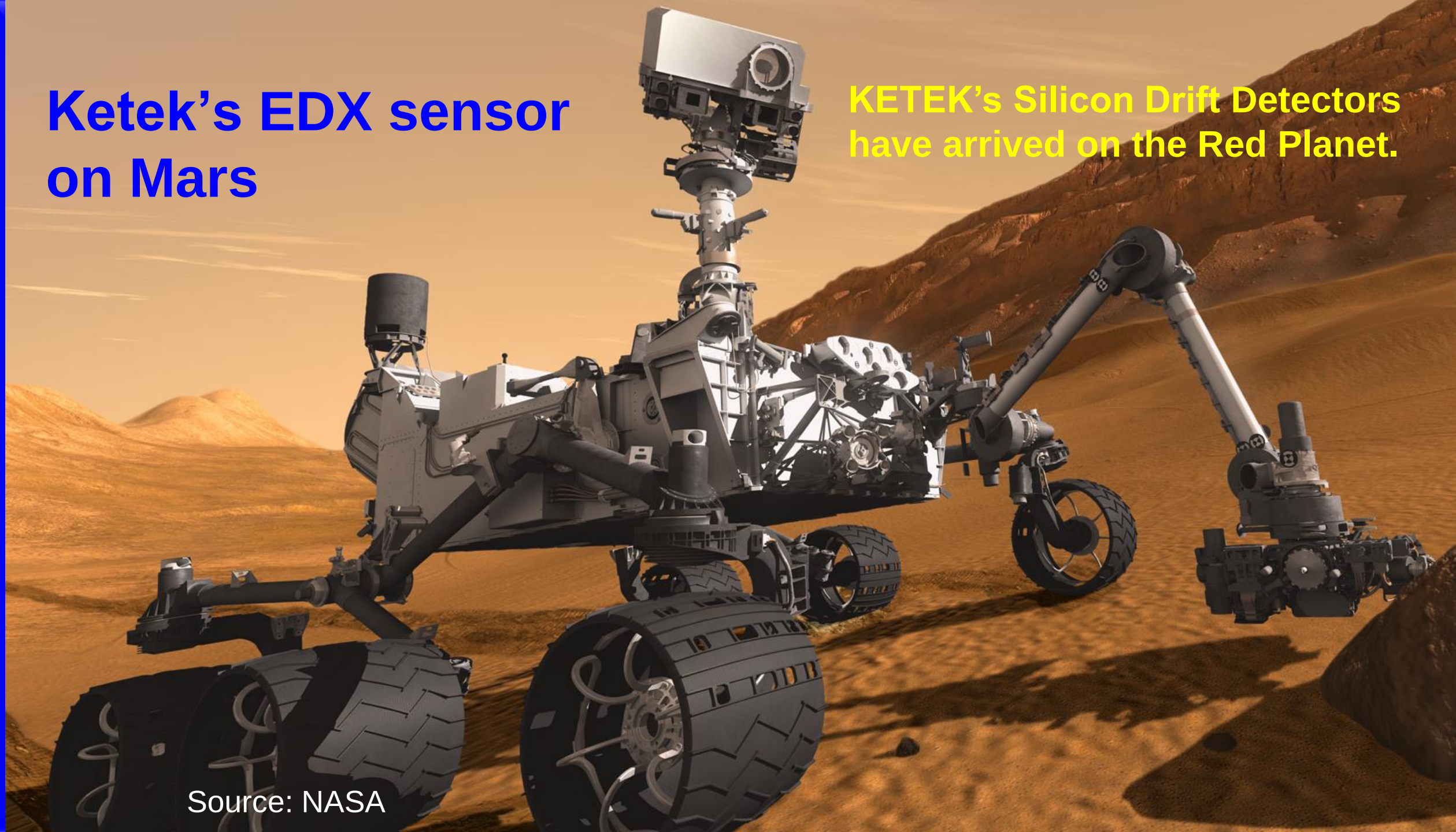
C-Si gets better after 100 M pulses!

C is superior to TiSi

(Max Stelzer et al., submitted)

Ketek's EDX sensor on Mars

KETEK's Silicon Drift Detectors have arrived on the Red Planet.



Source: NASA

A problem: Beryllium window (Be)

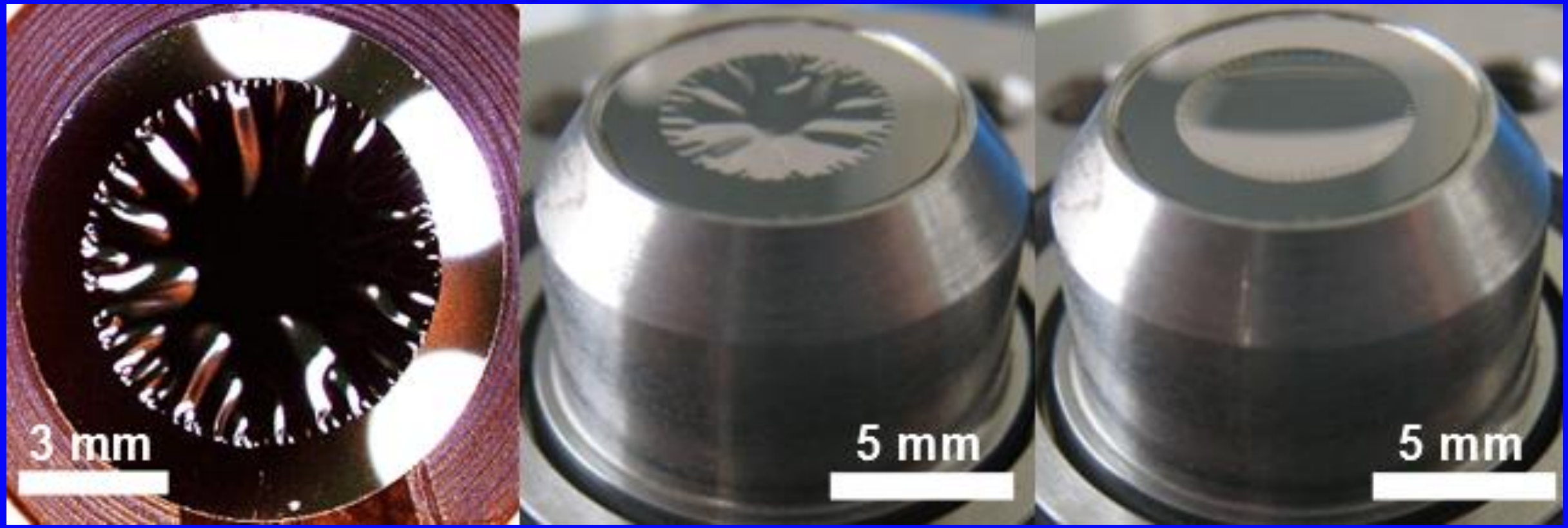
- only 2 suppliers
- very expensive
  ~ € 300
  or 500000 €/g
- very toxic material
- toxic waste
  if broken

diamond, SiN, polymers etc have been tried
…but all need a support grid and/or additional layers

Department of Hybrid Electronic Systems

Technische Universität München

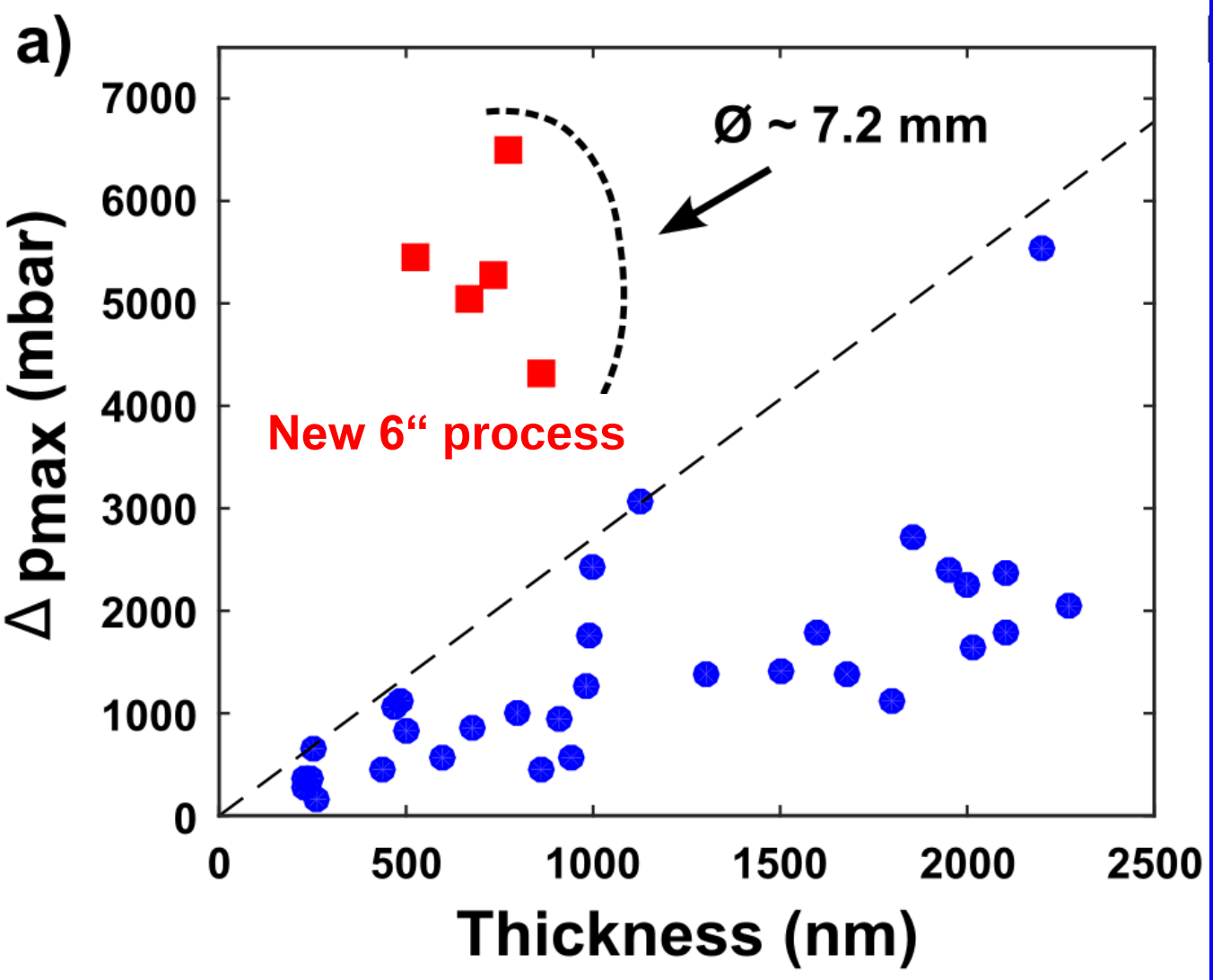
High Performance X-ray Transmission Windows Based on Graphenic Membranes



Sebastian Hübner et al., IEEE TNS 2015 10.1109/TNS.2015.2396116

Pressure stability tests

Sebastian Hübner et al., MRS Advances / March 2016

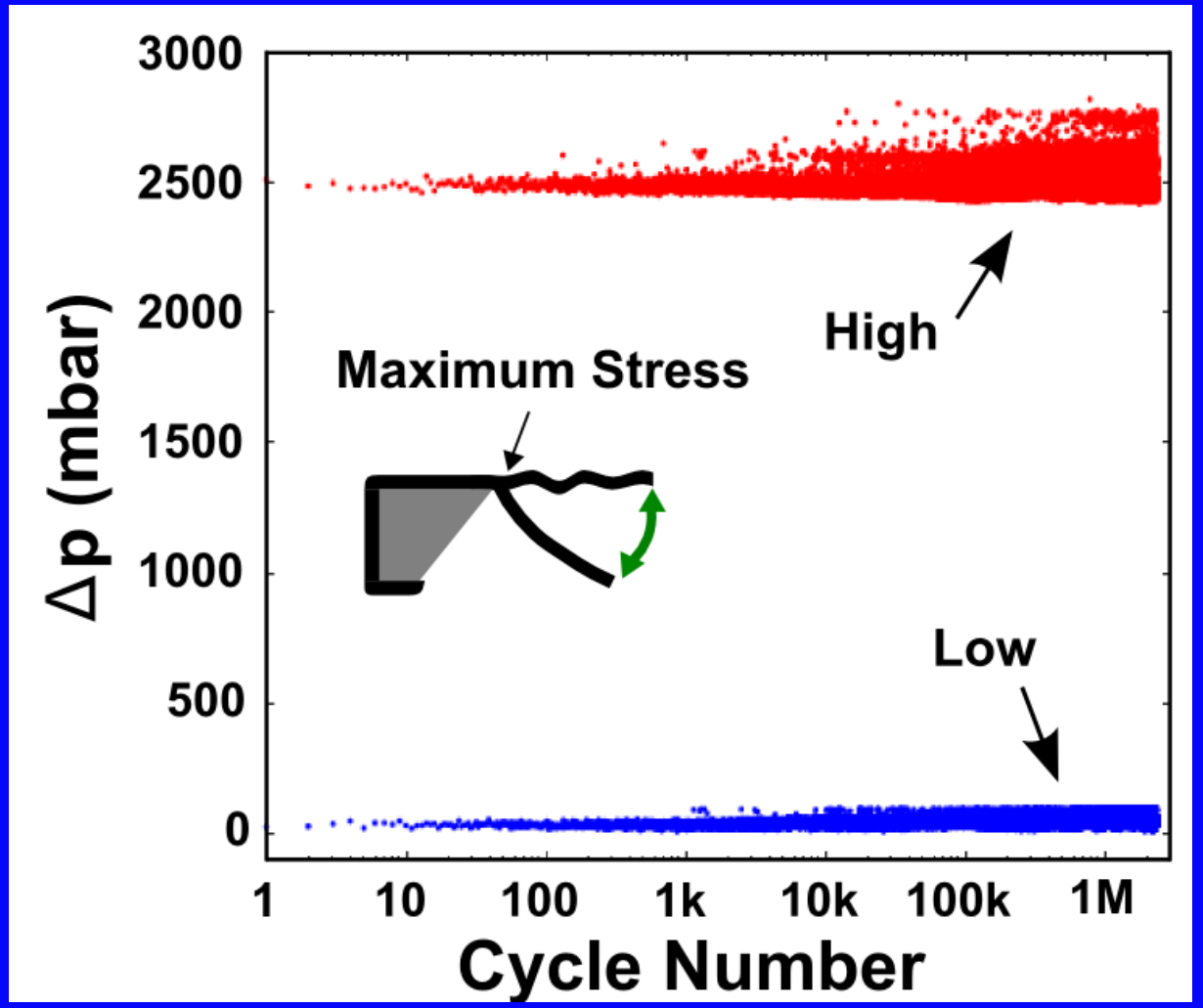


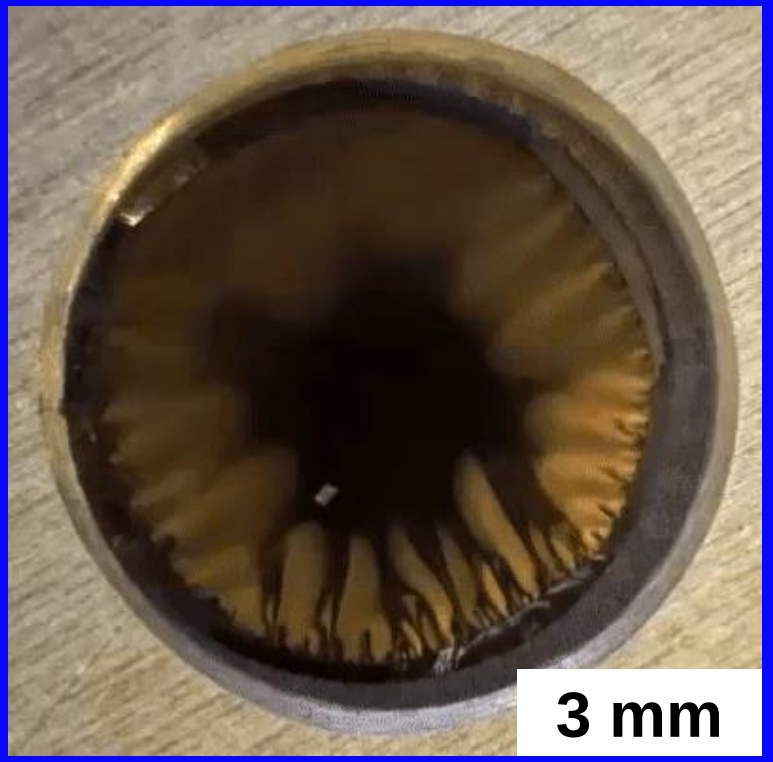
UTS = 7 GPa

0.6 µm thickness will hold Δp_{max} = 5 bar

Ultimate Tensile Strength

Pressure Cycle Stability



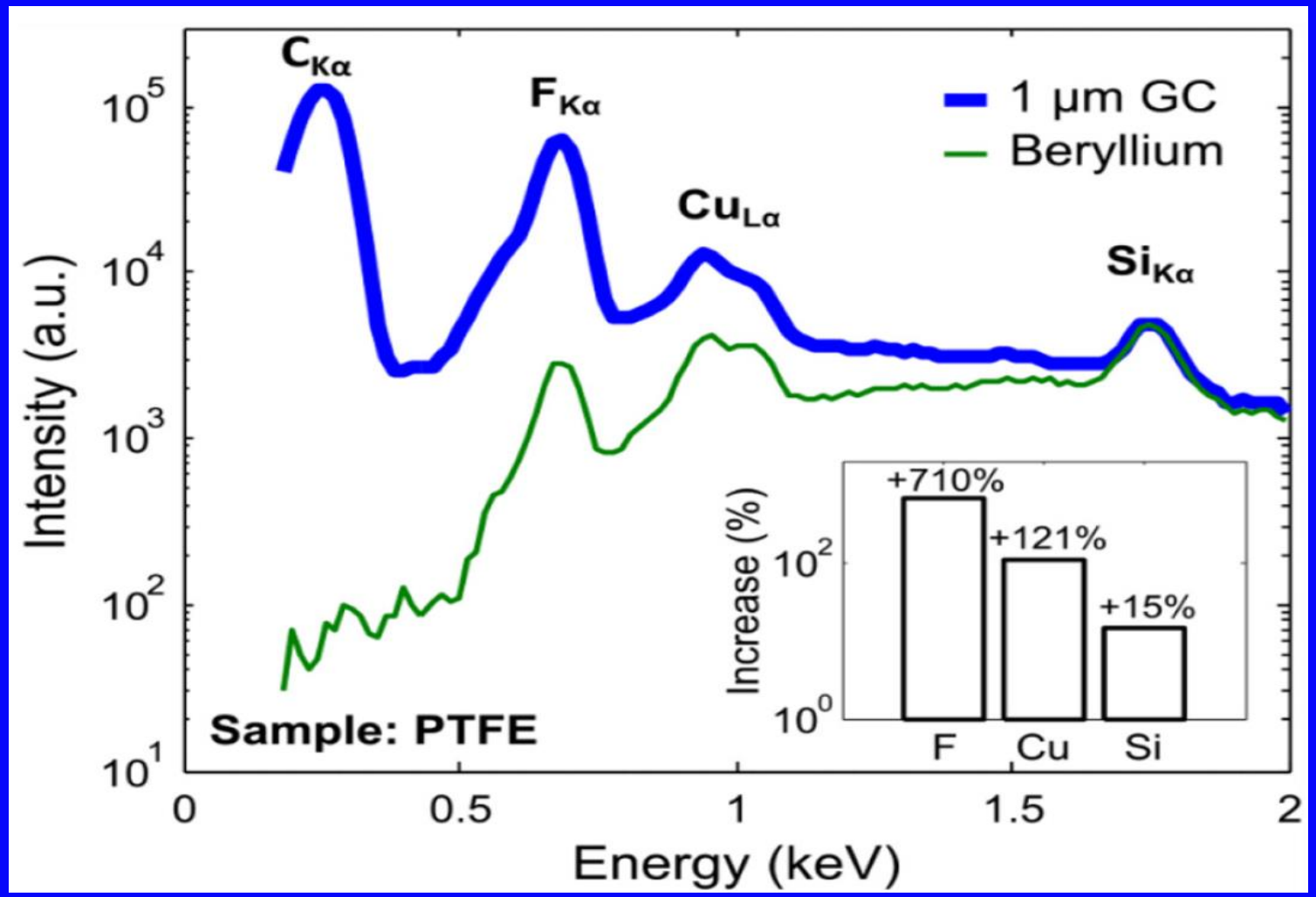


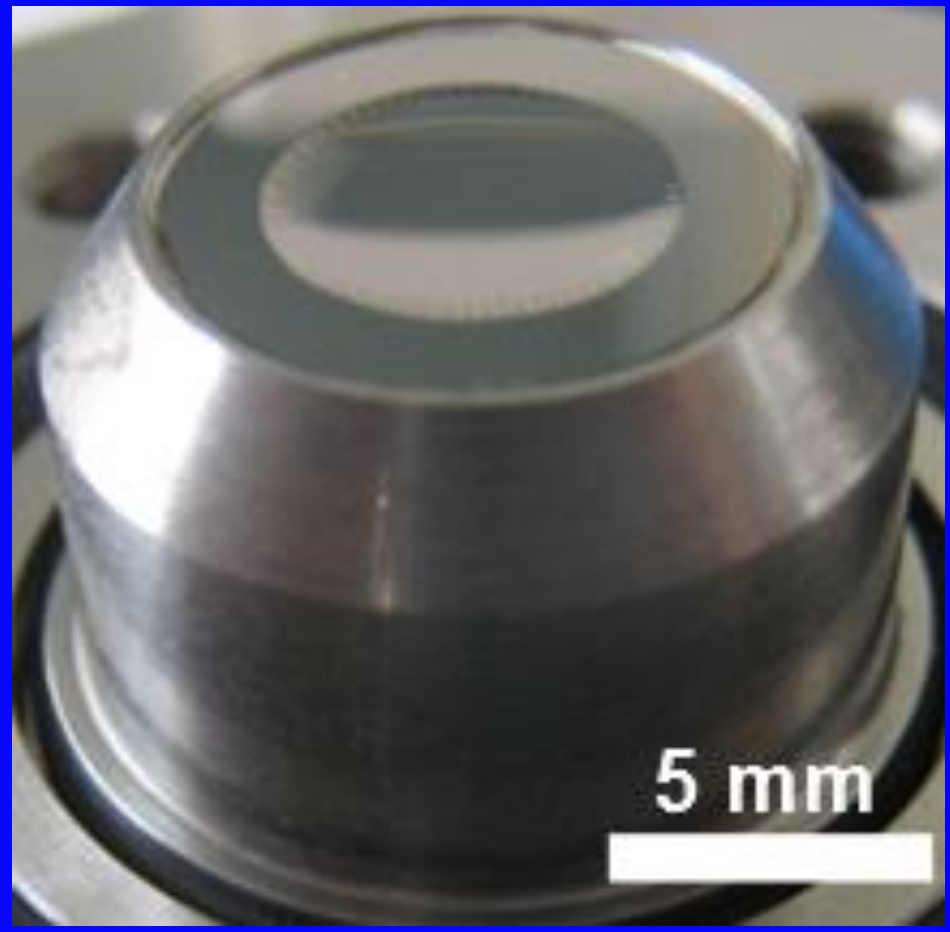
- Helium leak tight
  < 1×10^{-10} mbar L/s

Diameter 7.2 mm
Thickness 650 nm

High bending resilience

X-ray transmission evaluation

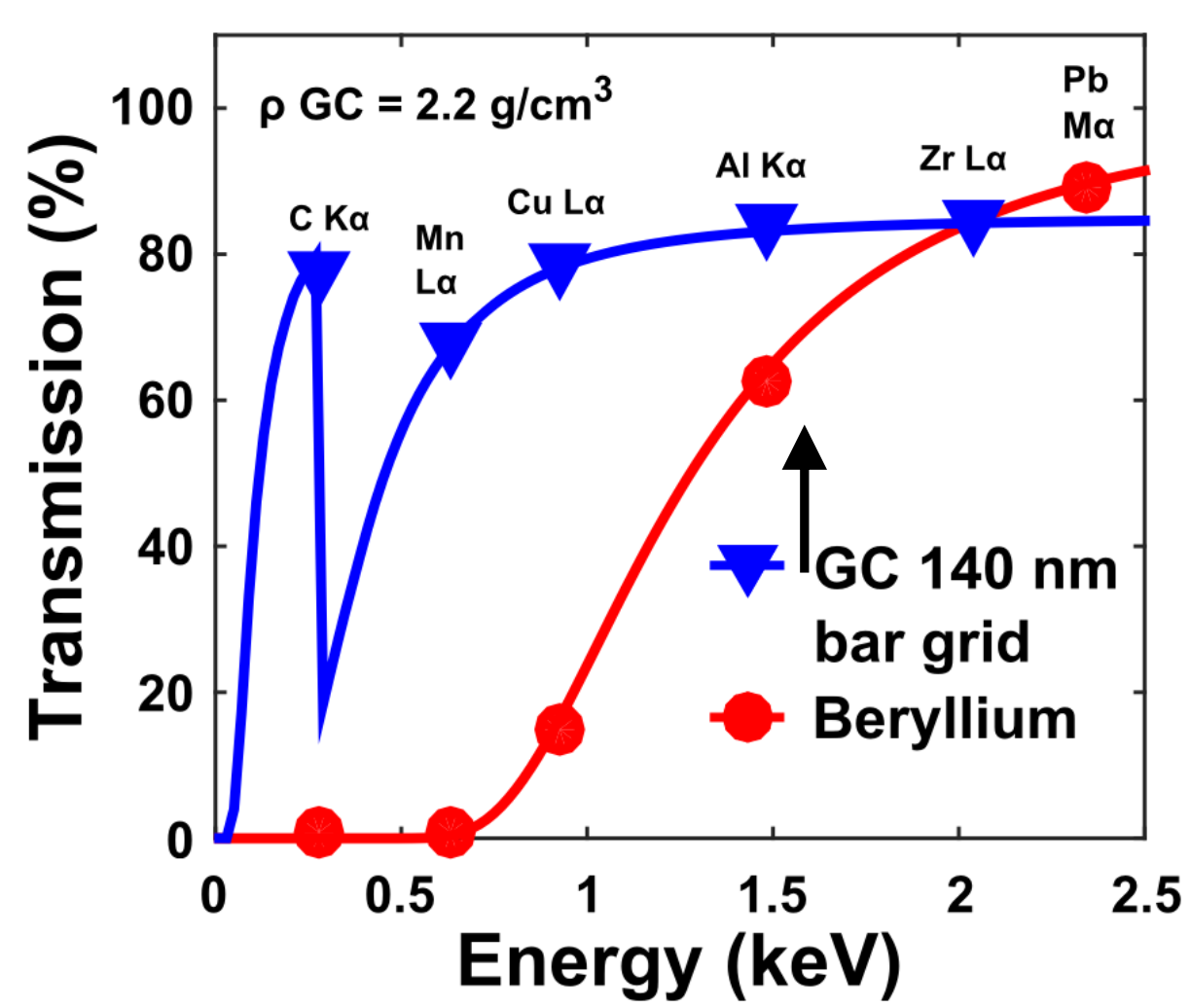


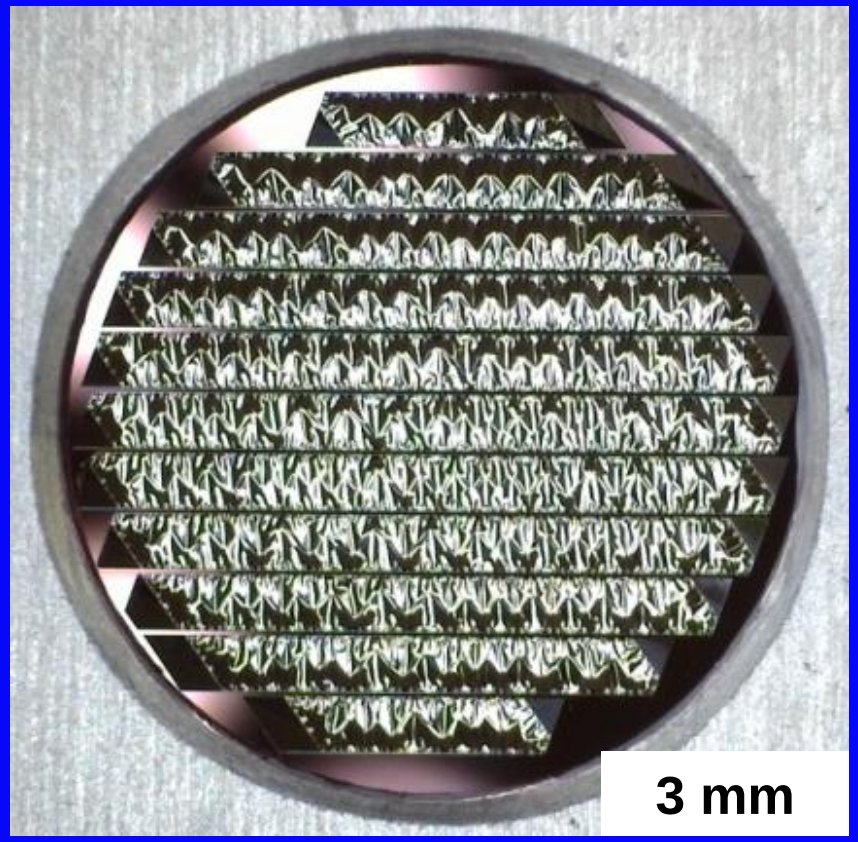


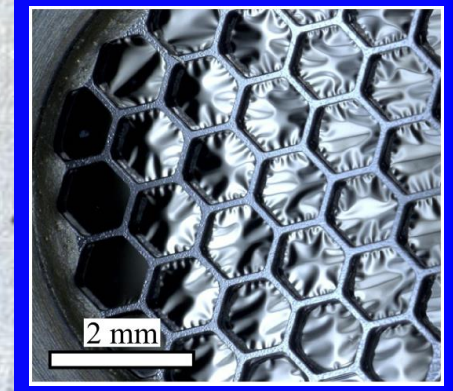
1 µm GC enables C, N, O and F detection

Sebastian Hübner et al., IEEE TNS 2015 10.1109/TNS.2015.2396116

Low X-ray Energy Window



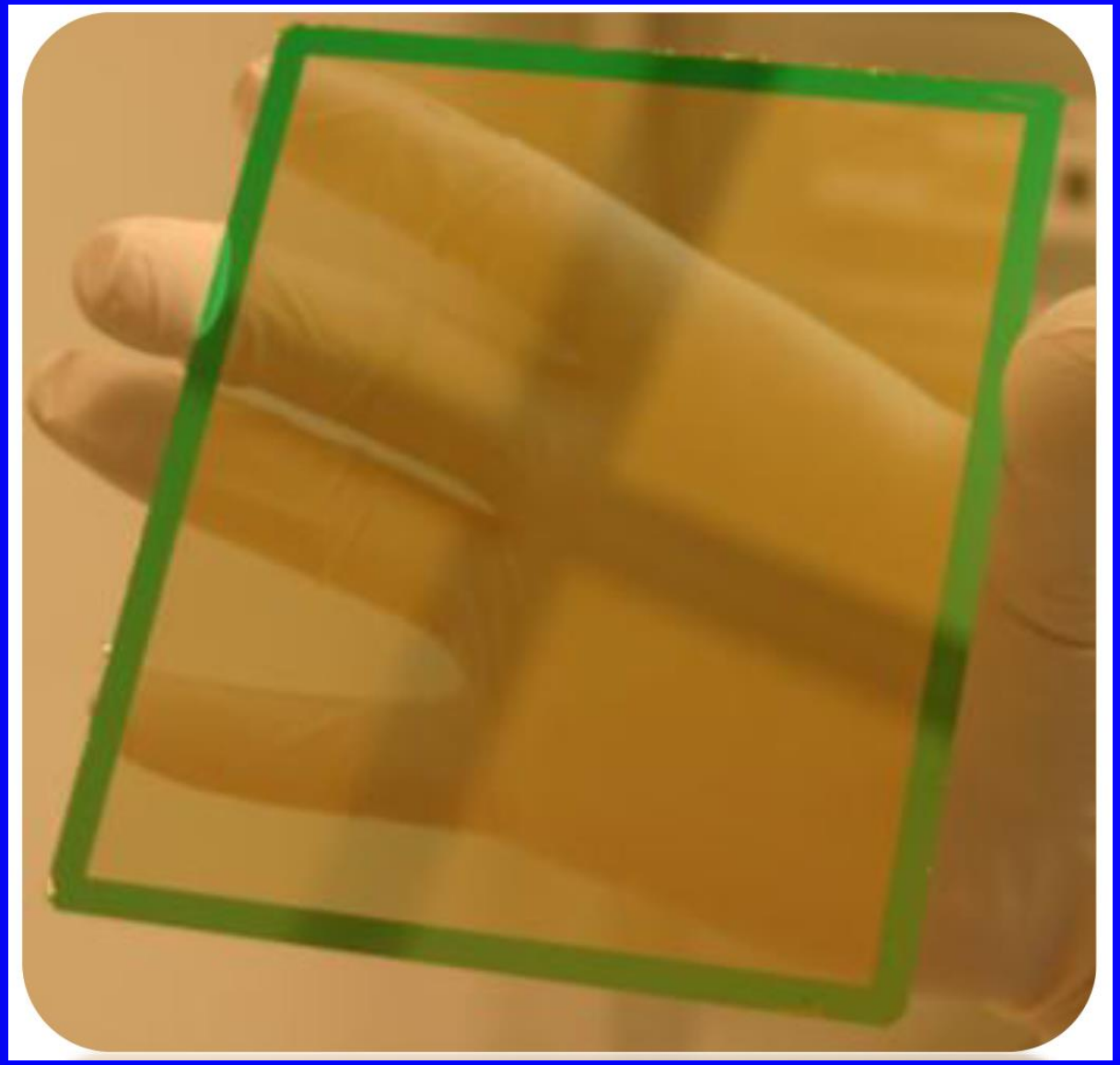


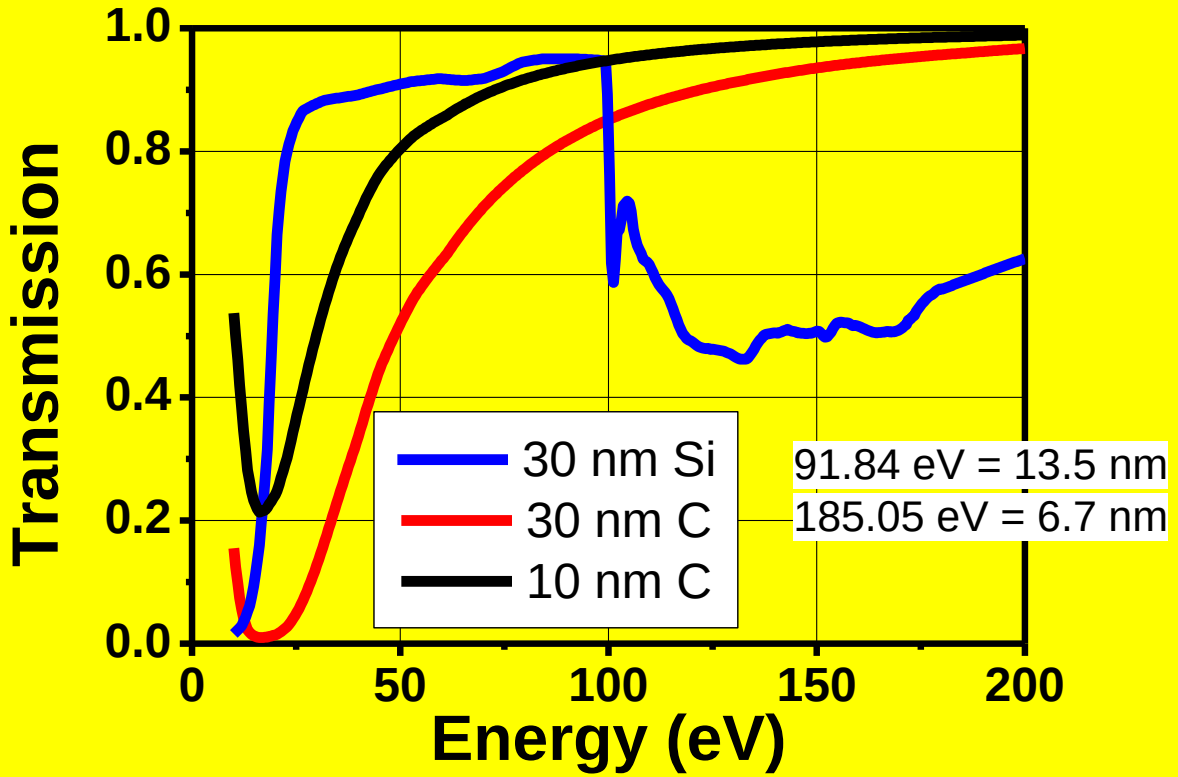


- High transmission for C, O and N detection
- Helium leak tight
- Fluorescent blind

High transmission below 2 keV!

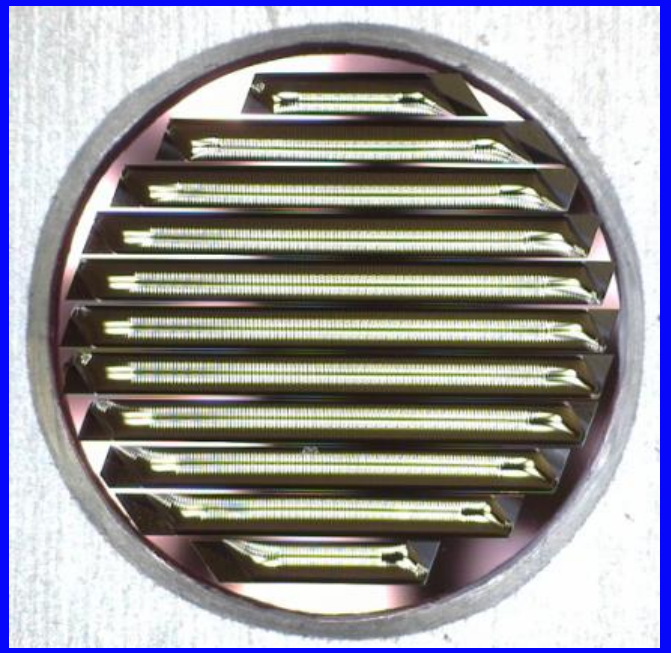
EUV pellicle for future (!) 6.7 nm node





ASML: Full size pSi pellicle realized, 103x122 mm, 85% (single pass) transmission

Successful implementation of graphenic carbon transmission windows for EDX and XRF



X-Ray Window Requirements	Beryllium	Graphenic Carbon
No Support Grid at 7 mm Opening Diameter	*Yes*	*Yes*
X-Ray Transmission	*71 % @ 1.5 keV*	*85 % @ 1.5 keV*
Pressure Stability > 2bar	*Yes*	*Yes*
Pressure Cycle Fatigue	*>20k cycles*	*>10M cycles*
Helium Leak Rate	*<1 x10^{-10} mbar L/s*	*<1 x10^{-10} mbar L/s*
Light Tight	*Yes*	*Yes*
Chemical Resistance	*High*	*High*
Non-Toxic	*No*	*Yes*
Availability/Supply	Limited	Unlimited

Huebner et al., MRS Advances 2016, 10.1557/adv.2016.194
Huebner et al., physica status solidi (b), 2015, 2564-2573
Hübner et al., IEEE TNS 2015

Summary

- Devices
  - Excellent: single-walled CNT FETs
  - How to realize products?
- Interconnects
  - Thru Silicon Vias
  - Capacitors (DRAM and passives)
  - Midgap gate material
  - Schottky-Diodes
- Sensors and Memories
  - X-ray windows
  - Carbon Memories
  - Spin filter
  - Photo-detectors

Questions and Comments?

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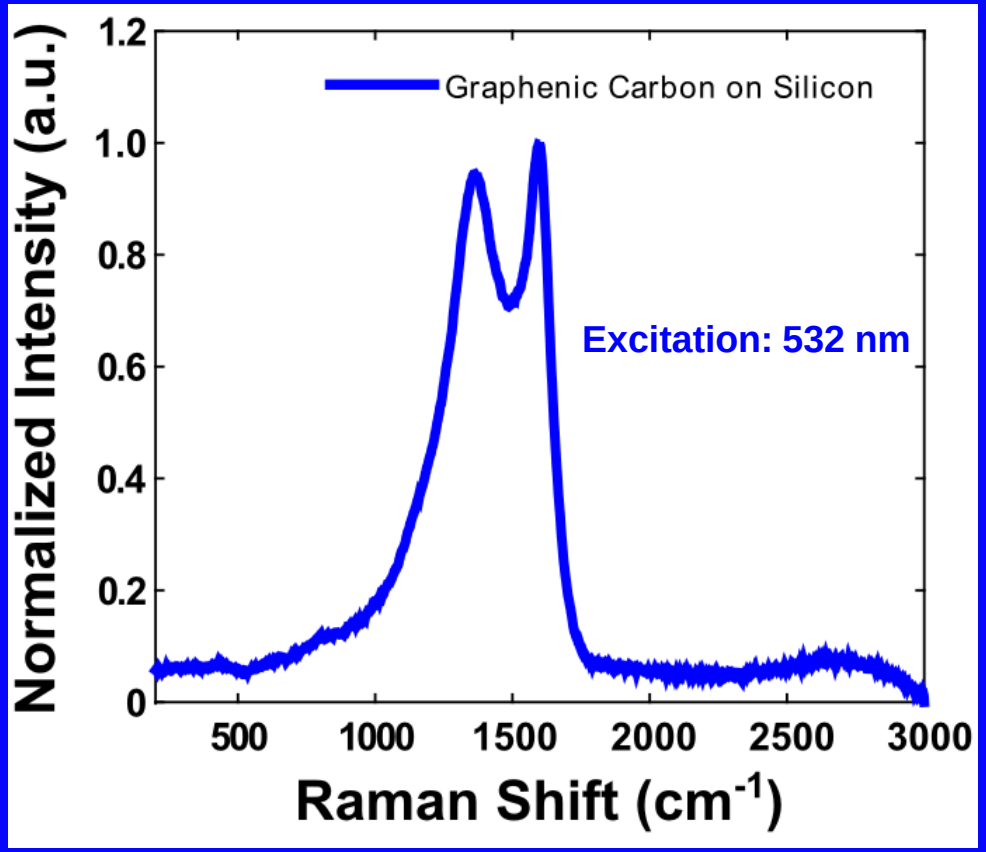
Properties of Graphenic Carbon

Properties	GC
Density	2.2 g/cm3
Resistivity	1 mΩ cm
Stress (on Si)	400–500 MPa
Young modulus	150 GPa
UTS	7 GPa



Carbon fiber (Toray T1000G)
(the strongest man-made fibres)
6.370 GPa fibre alone

- Carbon FET Devices
  - Nanotubes or Graphene & other 2D
  - Challenges
- Carbon Interconnects
  - DRAM Capacitors
  - Carbon-Silicon Schottky Diodes
  - Interconnects
- Graphenic Membranes
  - X-ray Transmission Windows
- Carbon-based Resistive Memories
- Photodetectors
- Carbon-based Spin-Filters