4th International Memory Workshop

May 20th – 23rd 2012

MELIA Milano, Milano, Italy

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Samsung	Intel	Micron
Korea	USA	Italy

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Giuseppe Crisenza, Micron, Italy
Jan Van Houdt, imec, Belgium
Pascal Mazoyer, ST Microelectronics, France
Tamer San, Texas Instrument, USA

Summary of Events

Sunday, 5/20

Registration	8:00AM - 4:00PM
Tutorial on System-Memory interactions	9:00AM – 12:00PM
Lunch Break (provided)	12:00PM -2:00PM
Tutorial on MRAM	2:00AM – 5:00PM

Monday, 5/21

Registration	7:00AM - 6:00PM
Opening remarks	8:00AM - 8:10AM
Session #1	8:20AM -11:50AM
Committee Luncheon Lunch (on your own)	12:00AM – 2:00PM
Session #2	2:00PM - 4:05PM
Panel discussion	4:30PM - 6:00PM
Poster Session	6:00PM – 8:00PM
Reception	6:00PM - 8:30PM

Tuesday, 5/22

Registration	7:00AM - 5:00PM
Session #3	8:00AM - 10:05AM
Session #4	10:25AM –12:05AM
Lunch Break (on your own)	11:40AM - 2:00PM
Session #5	2:00PM - 4:05PM
Session #6	4:25PM – 5:40PM
Banquet (provided)	7:00PM - 9:00PM

Wednesday, 5/23

Registration	7:00AM - 2:00PM
Session #7	8:00AM - 10:05AM
Session #8	10:25AM – 11:45AM
Lunch (provided)	11:45AM – 1:30PM
Session #9	1:30PM – 3:35PM
Session #10	3:55PM – 5:15PM
Closing Remarks	5:15PM- 5:45PM

Sunday May 20th, 2012

Tutorial Registration on site: 8:00AM - 4:15PM

Tutorial on System-Memory Interactions: 9:00AM – 12:00PM

Chair: Ken Takeuchi, Chuo University, Japan

9:00AM	Introduction	K. Takeuchi
9:10AM	NAND & Controller Co-design for SSD	K. Takeuchi
10:00AM	Break (Refreshments Provided)	
10:10AM	A Holistic View of Architecting Storage Class Memory into Future System	J. Li, IBM
11:00AM	High Performance Wireless Memory Interface Design	T. Kuroda, Keio Univ
11:50AM	Lunch break (Provided)	

Tutorial on MRAM: 2:00PM – 5:00PM

Chair: B, Dieny, CEA / Spintec, France

2:00PM	Introduction	B. Dieny, CEA/Spintec
2:10PM	Magneto-resistance, STT: Materials	S. Yuasa, AIST
3:00PM	SW-MRAM, Toggle MRAM, STT-RAM	D. Worledge, IBM
3:50PM	Break (Refreshments Provided)	
4:00PM	STT, Thermally assisted MRAM and hybrid CMOS/MTJ electronics	B. Dieny, CEA/Spintec

Conference location:
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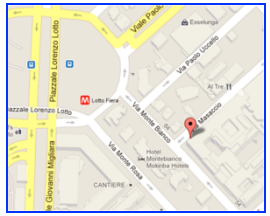

Poster Session

Monday May 21st, 2012 6:00 PM – 8:00 PM **POSTER PAPERS**

1) M. Boniardi, Micron, "Electrical and Thermal Behavior of Tellurium poor GeSbTe Phase Change Memory"
2) G. Palma, CEA-LETI-MINATEC, "Experimental investigation and empirical modeling of the set and reset kinetics of Ag-GeS2 CB Memories"
3) W.G. Kim, imec, "Effect of Inserting Al2O3 Layer and Device Structure in HfO2-based ReRAM for Low Power Operation"
4) A. Arreghini, imec, "Ultimate scaling projection of cylindrical 3D SONOS devices"
5) Q. Hubert, CEA, "Lowering the reset current and power consumption of Phase-Change Memories with carbon-doped Ge2Sb2Te5"
6) G. M. Paolucci, Dipartimento di Elettronica e Informazione, "Investigation of Cycling-induced VT Instabilities in NAND Flash Cells via Compact Modeling"
7) A. Hanada, "NIAIST, "High-Speed and Multi-Bit Resistive Switching Brought about by Migration of Hydrogen Ions in Resistive Random Access Memory Consisting of $Bi_2Sr_2CaCu_2O_8$ Single Crystal"
8) L. Masoero, CEA , "Physical understanding of program injection and consumption in ultra-scaled SiN Split-Gate memories"
9) G. Navarro, CEA, LETI, MINATEC, "Investigation of the Electrical Performances of trench PCM at High Operating Temperature"
10) W. Zhao, Univ Paris-Sud, "High Density Spin-Transfer Torque (STT)-MRAM based on Cross-Point Architecture"
11) Y. Jeong, Hynix, "A Investigation of E/W Cycle Characteristics for 2y-nm MLC NAND Flash Memory Devices"
12) E. Yurchuk, Namlab gGmbH, "HfO2-based Ferroelectric Field-Effect Transistors with 260 nm channel length and long data retention"
13) P. Lorenzi, Sapienza University of Rome, "Impact of forming pulse geometry and area scaling on forming kinetics and stability of the low resistance state in HfO2-based RRAM cells"
14) B. Park, Hynix, "An Investigation of Abnormal Program Phenomena with S/D Junctions and Dopant Profiles for Sub-20 nm NAND Flash Memory Devices"
15) C. Zhu, University, "High Performance MAHAHOS Memory Devices: Charge Trapping and Distribution in Bandgap Engineered Structure "
16) Y. Shuto, Tokyo Institute of Technology, "Static noise margin and power-gating efficiency of a new nonvolatile SRAM cell based on pseudo-spin-transistor arch."
17) P. Blomme, imec, "Scalability study of fully planarized hybrid floating gate Flash memory cells with high-k IPD"
18) A. Misra, IIT-B, "Large Memory Window Floating Gate Flash Memory with Multilayer Graphene as Charge Storage Layer."
20) M. Wang, University, "Study of One Dimension Thickness Scaling on Cu/HfOx/Pt Based RRAM Device Performance"
21) S.-W. Fang, eMemory Technology Inc, "A Dynamic Programming Method with Programming Current Clamped in Embedded P-Channel SONOS Flash Memory"
22) F. Gamiz, Nanoelectronics Laboratory, Department of Electronics, "3D Trigate 1T-DRAM memory cell for 2x nm nodes"

Monday May 21st, 2012

Registration 7:00 AM - 6:00 PM

Session #1 8:00 AM – 11:50 AM INVITED PAPERS

Chairs: Jundgal Choi, Samsung, Korea
Pranav Kalavade , Intel Corp, USA

8:00 AM Jungdal Choi, Opening Remarks
8:20 AM K. Prall, Micron, "An Update on Emerging Memory: Progress to 2Xnm"
8:50 AM S.-K. Lee, Hynix, "Technology Innovation for Scaling of NAND Flash Memory"
9:20 AM K. Baker, Freescale, "Embedded Nonvolatile Memories: A Key Enabler for Distributed Intelligence"
9:50 AM Break (Refreshments Provided)
10:20 AM Z. Wei, Panasonic, "Retention Model for High density RRAM"
10:50 AM K. Quader, SanDisk, "Flash Memory at a Cross-road: Challenges & Opportunities"
11:20 AM S. Lee, BeSang, "Architecture of 3D Memory Cell Array on 3D IC"

11:50 AM - 2:00 PM Lunch Break (on your own)

12:00 PM Committee Luncheon

Session #2 2:00 PM – 4:05 PM NAND + 3D

Chairs: Aochi, Hideaki, Toshiba
T. C. Lu, Macronix, Taiwan

2:00 PM K. P. Chang, Macronix, "An efficient Architecture for 3D vertical gate NAND flash using plural Island-gate SSL Decoding and study of its inhibit characteristics"
2:25 PM S.-T. Ahn, Hynix, " Advanced hot carrier injection programming scheme for sub-20nm NAND flash cell and beyond"
2:50 AM P. Poliakov , Katholieke Universiteit Leuven, "Spacer-Defined EUV Lithography Reducing Variability of 12nm NAND Flash Memories"
3:15 PM H. Huh, Hynix, "A 64Gb NAND Flash Memory with 800MB/s Synchronous DDR Interface"
3:40 PM M.-S Seo, Tohoku University, "Highly Scalable 3-D Vertical FG NAND Cell Arrays Using the Sidewall Control Pillar (SCP)"

4:05 PM Break (Refreshments Provided)

Panel discussion 4:30 PM – 6:00 PM

"**Future Memory Leader: MRAM or RRAM?**"

Panelists: Robert Aitken, ARM; Bernard Dieny, CEA/Spintec; Franz Kreupl, Technische Universitaet Muenchen; Kirk Prall, Micron; Daniel Worledge, IBM
Moderator : Raman Achutharaman, Applied Materials, Inc., USA
Sponsor : Applied Materials, Inc., USA

Poster Session : 6:00 PM – 8:30 PM
Chairs: Gill Lee, Applied Materials, USA

6:00 PM Poster Introduction
(See the front page for the list of poster papers)

Reception /Banquet 6:00 PM - 8:30 PM
Sponsor : Applied Materials, Inc., USA

Tuesday May 22nd, 2012

Registration 7:00 AM - 5:00 PM

Session #3 8:00 AM - 10:05 AM RRAM-1

Chairs: Gabriel Molas, CEA LETI, France
Damien Deleruyelle, Aix-Marseille University, France

8:00 AM A. Fantini, imec, "Intrinsic switching behavior in HfO_2 RRAM by fast electrical measurements on novel 2R test structures"
8:25 AM B. Butcher, Sematech, "Hot forming to improve memory window and uniformity of low-power HfOx-based RRAMs"
8:50 AM S. Larentis, Dipartimento di Elettronica e Informazione, "Bipolar-switching model of RRAM by field- and temperature-activated ion migration"
9:15 AM D. C. Gilmer, Sematech, "Asymmetry, Vacancy Engineering and Mechanism for Bipolar RRAM"
9:40 AM J. Liang, Stanford University, "Scaling Challenges for the Cross-point Resistive Memory Array to Sub-10nm Node – An Interconnect Perspective"
10:05 AM Break (Refreshments Provided)

Session #4 10:25 AM – 12:05 AM MRAM+FRAM

Chairs: Takayuki Kawahara, Hitachi, Japan
Bernard Dieny, CEA/Spintec, France

10:25 AM B. Lacoste, Spintec, "Sub-nanosecond Precessional Switching in a MRAM Cell with a Perpendicular Polarizer"
10:50 AM D. C. Worledge, IBM , "Recent Advances in Spin Torque MRAM"
11:15 AM S.Amara, Spintec, "Barrier Breakdown mechanisms in MgO-based Magnetic Tunnel Junctions under pulsed conditions"
11:40 AM S. A. Qidwai, Texas Instruments, "A 48 Mhz. 64kB FRAM Optimized for Ferroelectric Domain Polarization"

12:05 AM - 2:00 PM Lunch Break (on your own)

Session #5 2:00 PM – 4:05 PM NAND + 3D

Chairs: Koji Sakui, Micron, Japan
Geert Van den bosch, imec, Belgium

2:00 PM C.H. Lee, Samsung, "Physical Modeling and Analysis on Improved Endurance Behavior of P-Type Floating Gate NAND Flash Memory"
2:25 PM Y. Yanagihara, University of Tokyo, "Control Gate Length, Spacing and Stacked Layer Number Design for 3D-Stackable NAND Flash Memory"
2:50 PM D.-H. Lee, Samsung, "A new cell-type string select transistor in NAND flash memories for under 20nm node"
3:15 PM P. Blomme, imec, "Monocrystalline Floating Gate structure for ultimate NAND flash scaling towards the 12nm node"
3:40 PM K.-S. Shim, Hynix, "Inherent Issues and Challenges of Program Disturbance of 3D NAND Flash Cell"
4:05 PM Break (Refreshments Provided)

Session #6 4:25 PM -5:40 PM DRAM

Chairs: David Gilmer, SEMATECH, USA

4:25 PM T. Atsumi, Semiconductor Energy Laboratory Co, "DRAM Using Crystalline Oxide Semiconductor for Access Transistors and not Requiring Refresh for More Than Ten Days"
4:50 PM M.-S. Kim, imec, "Understanding of Trap-Assisted Tunneling current - assisted by oxygen vacancies in RuOx/SrTiO3/TiN MIM capacitor for the DRAM Application"
5:15 PM J.-S. Park, Hynix, "Mobility Enhancement of Peripheral PMOSFET Using e-SiGe Source and Drain in sub-50nm DRAM"

Banquet 7:00 PM - 9:00 PM (provided)

Wednesday May 23rd, 2012

Registration 7:00 AM - 2:00 PM

Session #7 8:00 AM – 10:05 AM RRAM-2

Chairs: Ken Takeuchi, Chuo University, Japan
Jing Li, IBM, USA

8:00 AM Y. Wu, Stanford University, "AlOx-based Resistive Switching Device with Gradual Resistance Modulation for Neuromorphic Device Application"
8:25 AM J.F. Kang, Institute of Microelectronics, "Oxide-Based RRAM: A Novel Defect-Engineering- Based Implementation For Multilevel Data Storage"
8:50 PM K.Higuchi, Univ. Tokyo, "Investigation of Verify-Programming Methods to Achieve 10 Million Cycles for 50nm HfO2 ReRAM"
9:15 AM S. Choi, Politecnico di Milano-IU.NET, "Resistance drift model for conductive-bridge (CB) RAM by filament surface relaxation"
9:40 AM A. Padovani, Università di Modena e Reggio Emilia, "Understanding the Role the Ti Metal Electrode on the Forming of HfO2-based RRAMs"
10:05 AM Break (Refreshments Provided)

Session #8 10:25 AM – 11:45AM ENVM

Chairs: Michiel van Duuren, NXP, Netherlands
Chandu Gorla, SanDisk, USA

10:25 AM S.-T. Kang, Freescale, "Nanocrystal eFlash Memories - Extended Endurance of High Performance Embedded Microcontrollers and Scaling Capability"
10:50 AM S.M. Kim, University of California, "Flexible and Transparent Memory - Non-volatile memory based on graphene channel transistor for flexible and transparent electronics applications"
11:15 AM D. Shum, Infineon , "Highly Reliable Flash Memory with Self-aligned Split-gate Cell Embedded into High Performance 65nm CMOS for Automotive & Smartcard Applications"

11:45 AM – 1:30 PM Lunch (provided)

Session #9 1:30 PM – 3:35 PM PRAM

Chairs: Jing Li, IBM, USA
Gabriel Molas, CEA LETI, France

1:30 PM H. Pozidis, IBM, "A Framework for Reliability Assessment in Multilevel Phase-Change Memory"
1:55 PM K. Yoshioka, University of Tokyo, "High Density NAND Phase Change Memory with Block-Erase Architecture to Compromise Write and Disturb Requirements"
2:20 PM N. Ciocchini, Politecnico di Milano-IU.NET, "Modeling of threshold voltage drift in phase change memory (PCM) devices"
2:45 PM M. Suri, CEA-LETI-MINATEC, "Interface Engineering of PCM for Improved Synaptic Performance in Neuromorphic Systems"
3:10 PM A. Calderoni, Micron, "Investigation of Over-Reset programming in Phase Change Memory"
3 :35 PM Break (Refreshments Provided)

Session #10 3:55 PM -5:15 PM Novel Memory Solutions

Chairs: Yakov Roizin, TowerJazz, Israel

4:00 PM W. Kwon, Univ. of California, "Electro-Mechanical Diode Performance and Scaling for Cross-Point Non-Volatile Memory Arrays"
4:25 PM T. Saito, Center for Microelectronic Systems"Ratio-less 10-Transistor Cell and Static Column Retention Loop Structure for Fully Digital SRAM Design"
4:50 PM J. Jantunen, Nokia, "Dual-interface memory for RF memory tag systems"

5:15 PM – 5:45 PM Closing Remarks & Adjourn