

# Carbon / high-k Trench Capacitor for the 40nm DRAM Generation

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# Outline of Presentation

- Motivation
- Properties of Pyrolytic Carbon
- Integration for the DRAM Capacitor
- Electrical Results
- Summary

# Carbon as new FEOL Material

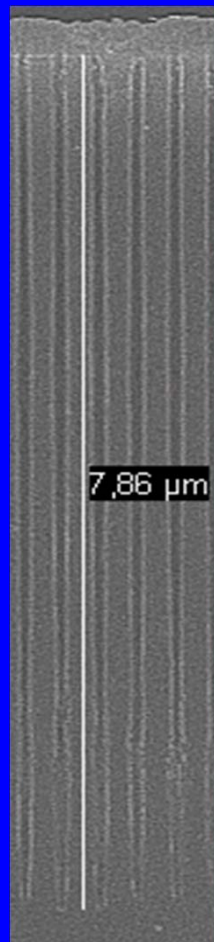
- Alternative to metals like TiN and TaN

- Possible Applications:

- Gate, Contacts, Interconnects,
- Stress Layer
- Sacrificial and Mold Material
- ...

→ Capacitor Electrode in DRAM

# Trench Capacitor Road Map



## Carbon Option

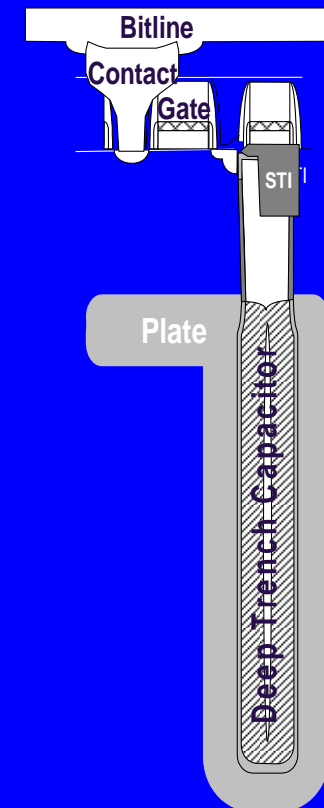
110nm	90nm	75nm	58nm	48nm
NO	NO	NON	NON / High-k	High-k
SIS	SIS	SIS	SIS / MIS	MIS / MIM

Trench Surface Enhancement

Trench Aspect Ratio

Metal

high-k



Shrink Generation

SIS...Si Insulator Si / MIS...Metal Insulator Si / MIM...Metal Insulator Si

# Benefits of Carbon

- High Conductivity
- High Temperature Stability
- Integration with NON and high-k viable
- Fills High Aspect Ratios
- Low Cost Pre-Cursors ( $C_xH_y$ )
- Easily structurable ( $O_2$ ,  $H_2$ )

# Outline of Presentation

- Motivation

- **Properties of Pyrolytic Carbon**

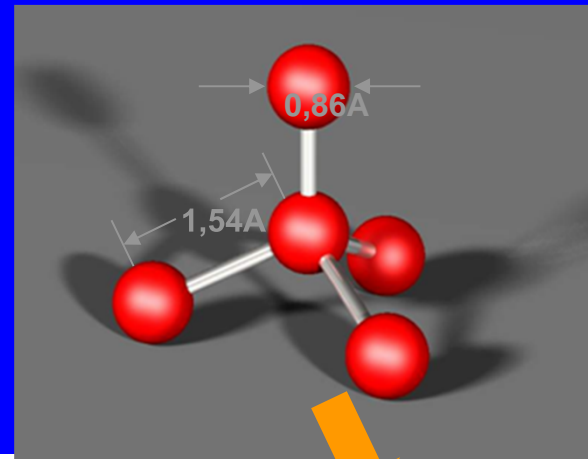
- Integration for the DRAM Capacitor

- Electrical Results

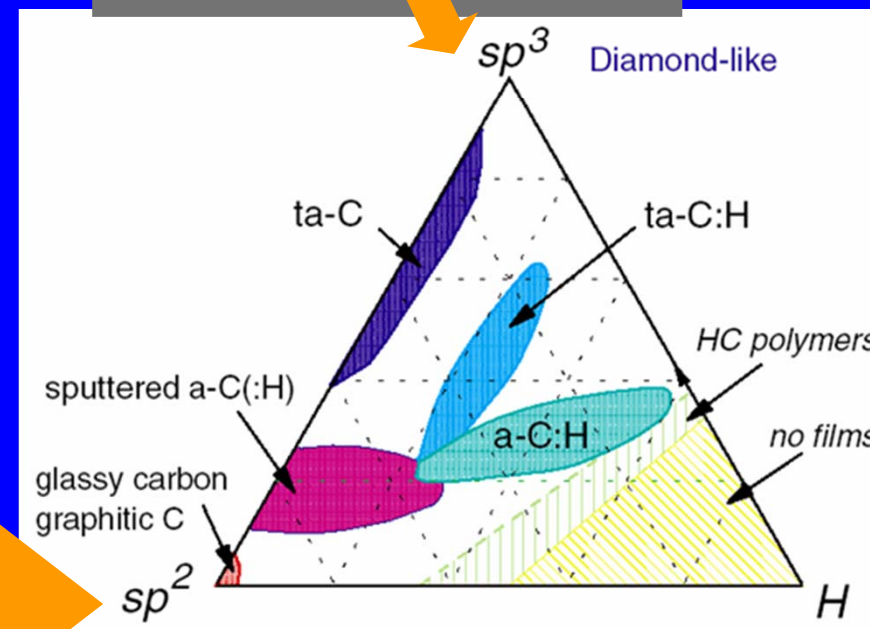
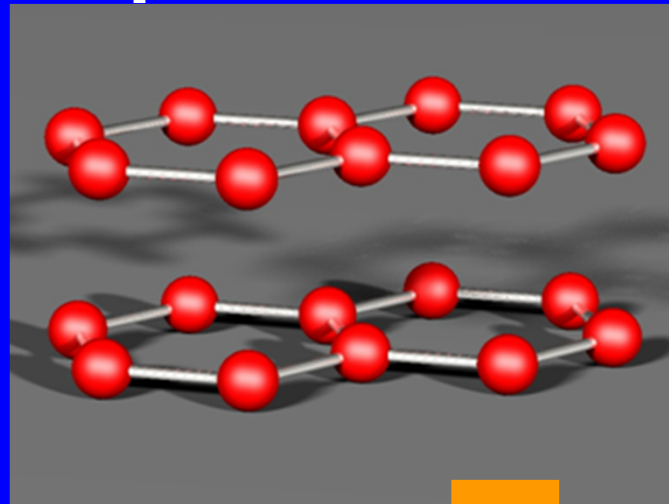
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# Structural

## Diamond

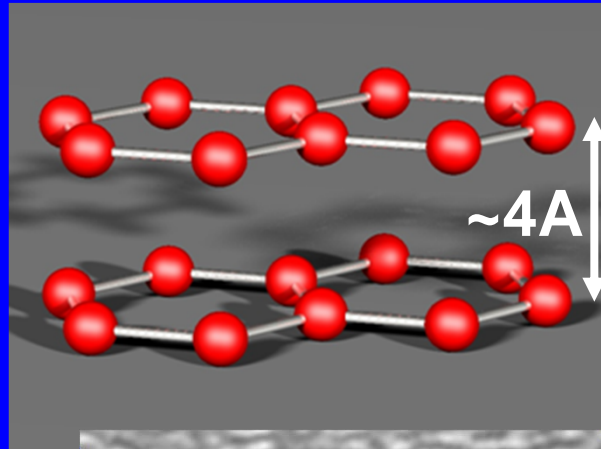


## Graphene Sheets

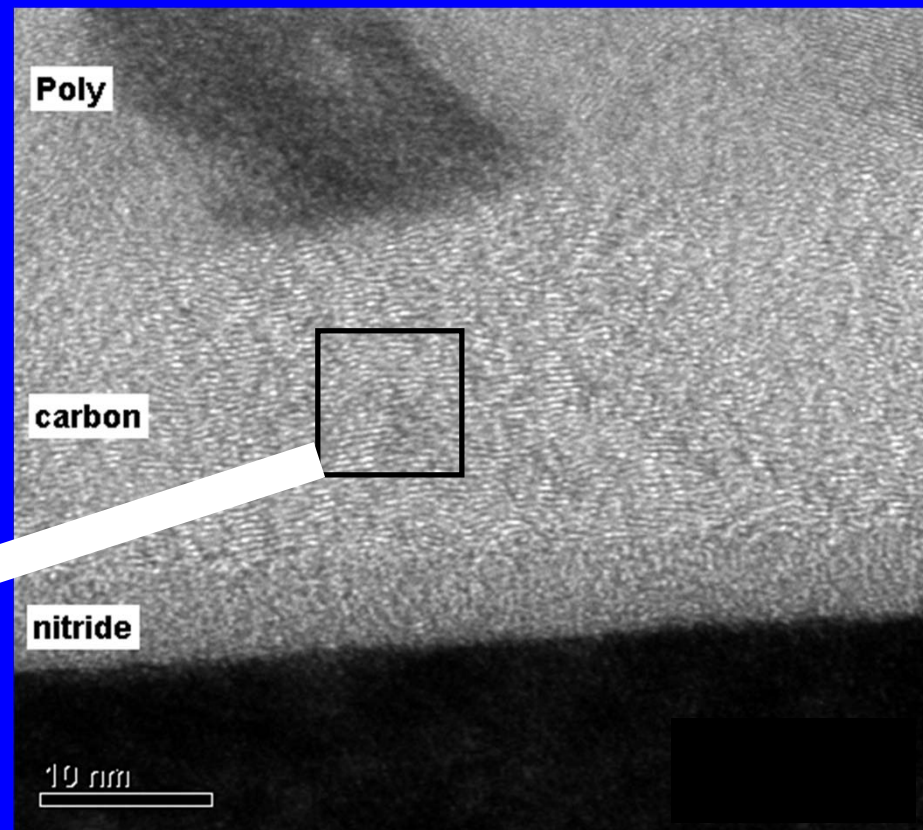
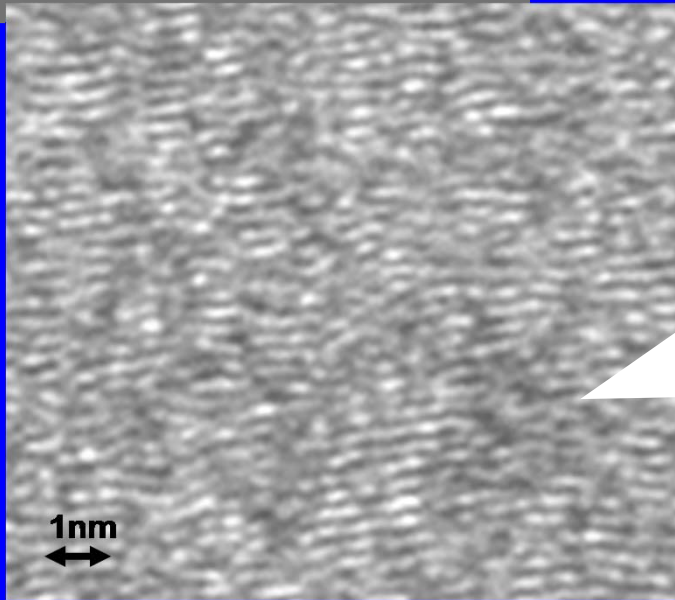


Desired material is the highly conductive Graphene

# Structural



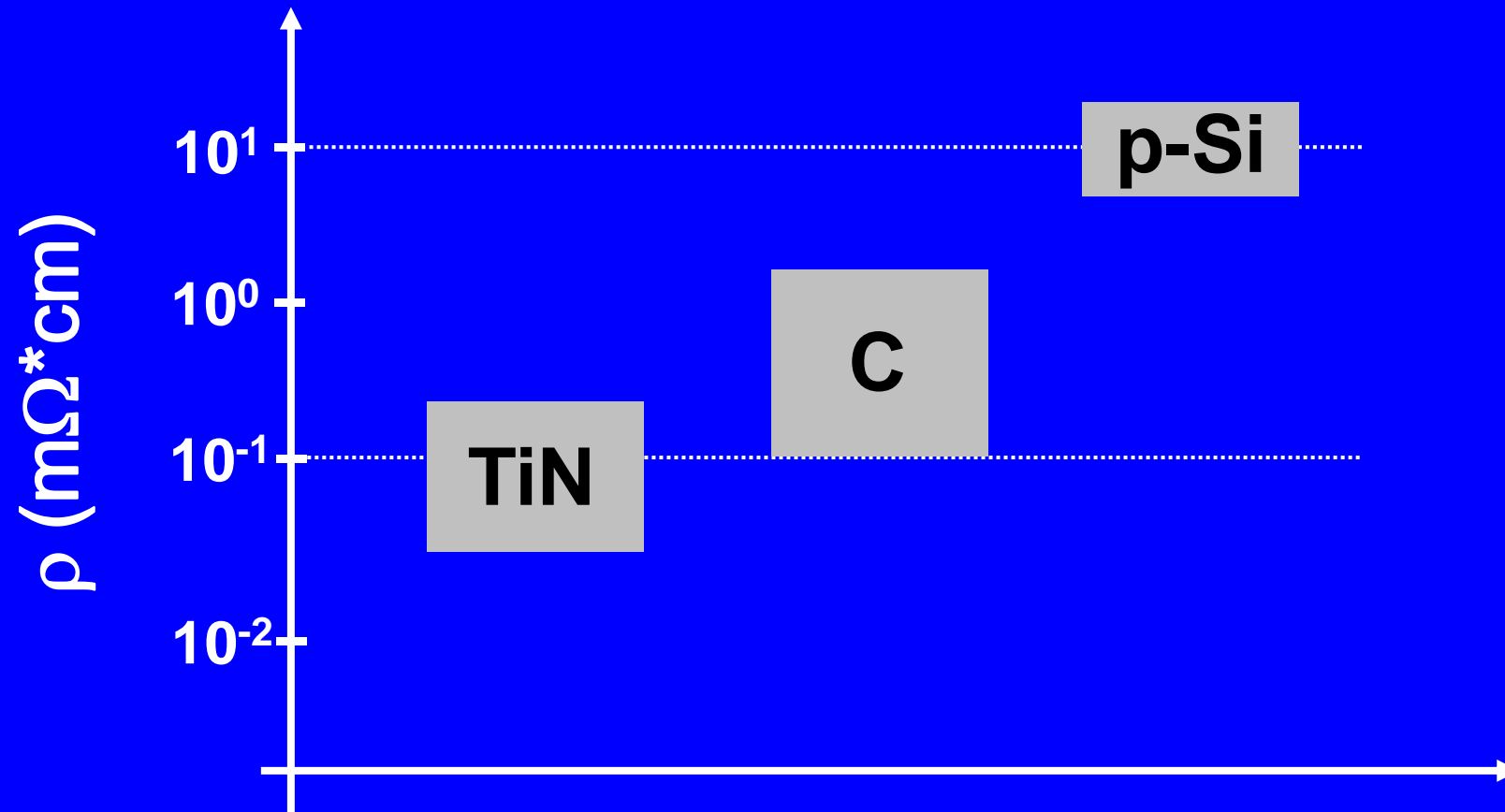
## Crystallites with layered structure



High conductivity along the layers



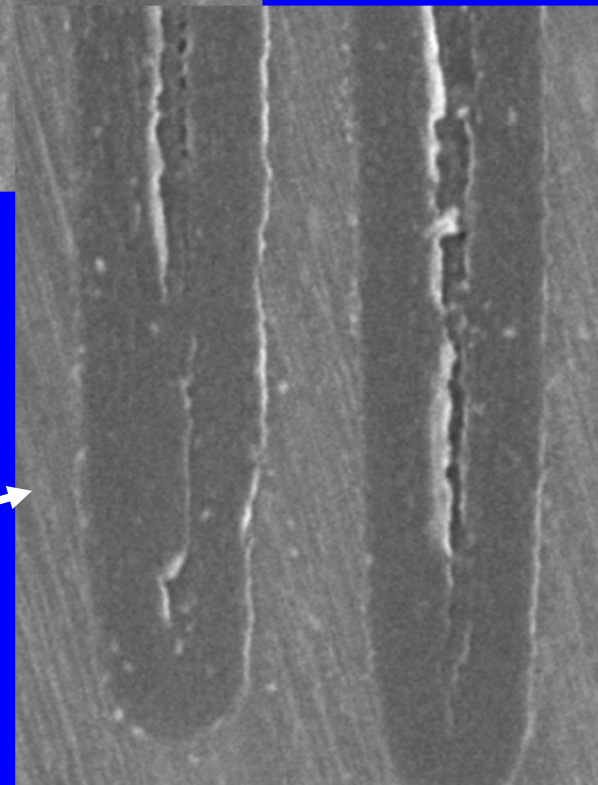
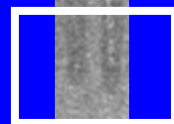
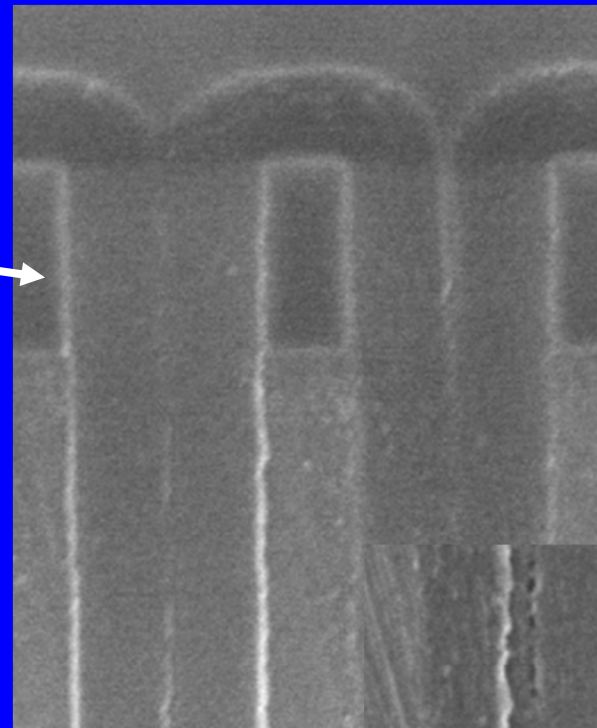
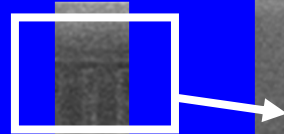
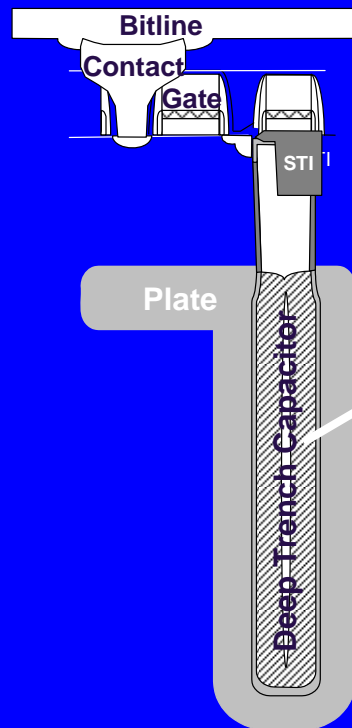
# Electrical Resistivity



Carbon resistivity can be as low as that of TiN

# Deposition

Nearly 100%  
step coverage  
in trench



# Carbon vs. TiN

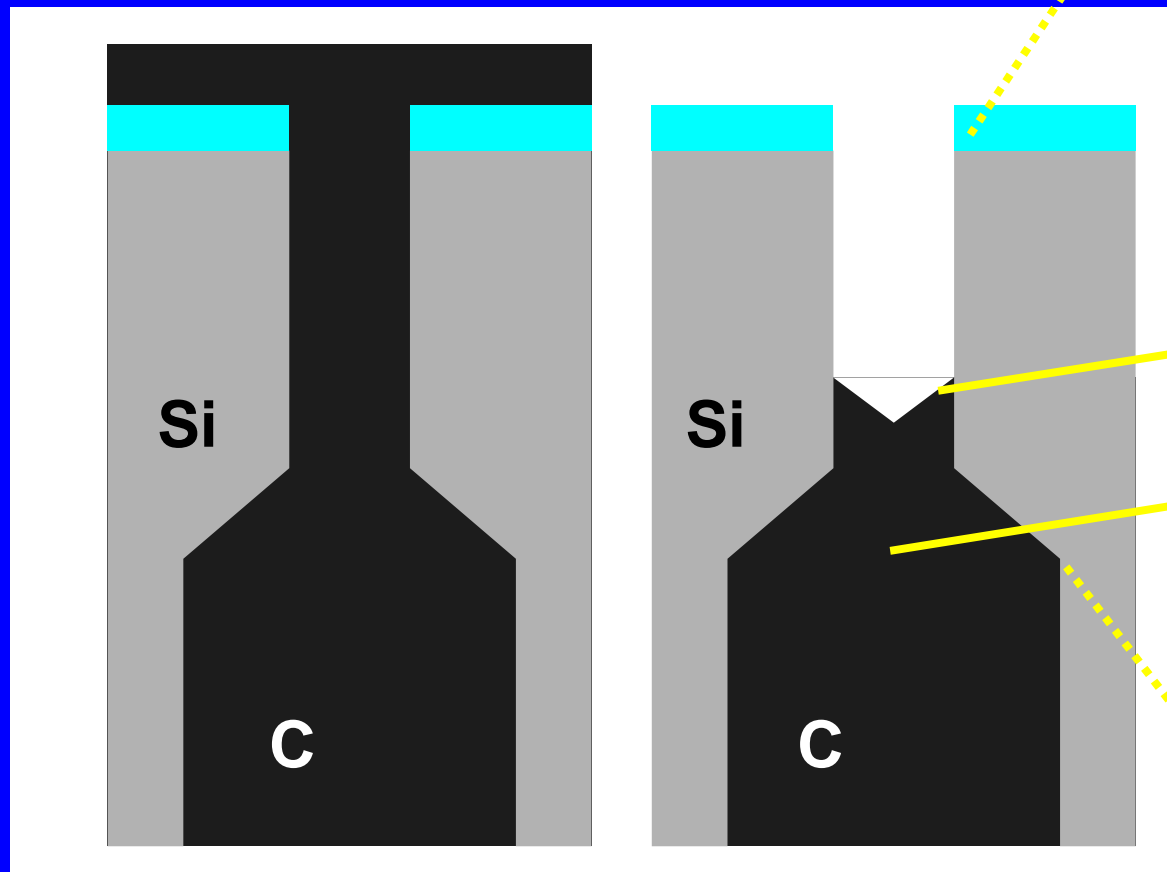
	Metal (TiN)	Carbon
$\rho$ ( $\mu\Omega\cdot\text{cm}$ )	50-200	120-2000
Max. AR shown	1:120	1:430
Step coverage	>85%	>95%
Process	pulsed CVD	LPCVD / RTP
Precursor	$\text{TiCl}_4$	$\text{C}_x\text{H}_y$
Rate (nm/min)	1-2	0.2 - 120
Thermal stability	>1200°C	>1200°C

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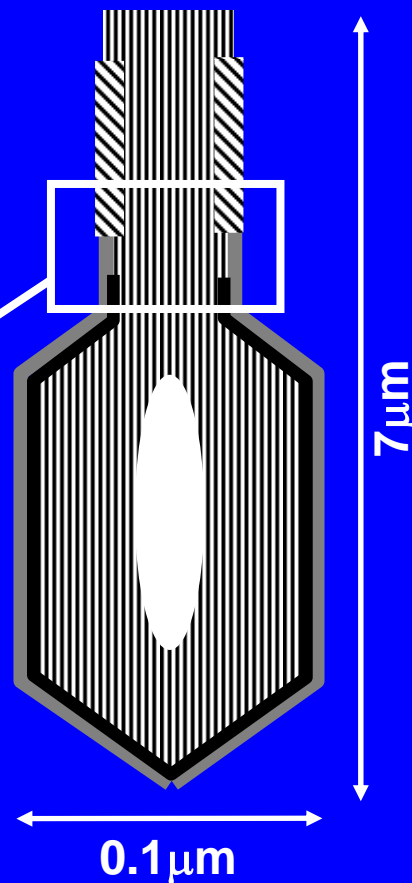
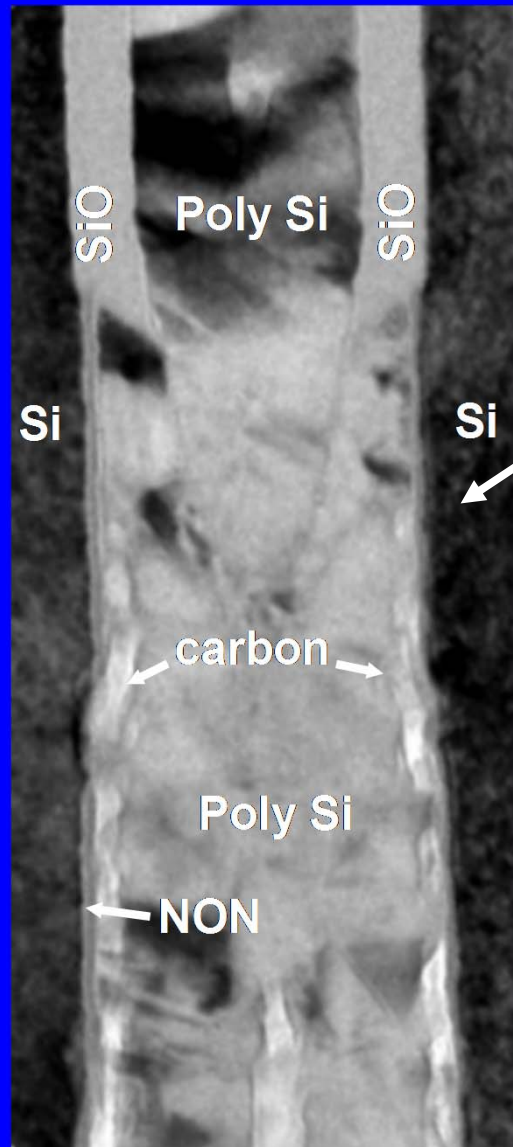
# Etch

- Dry etch by  $O_2$  and  $H_2$  Plasma

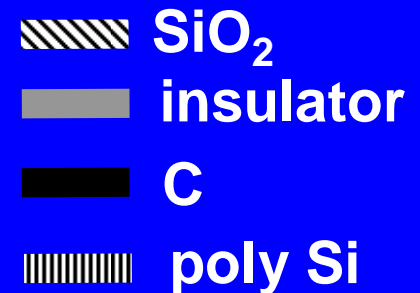


- No attack by wet chemistries

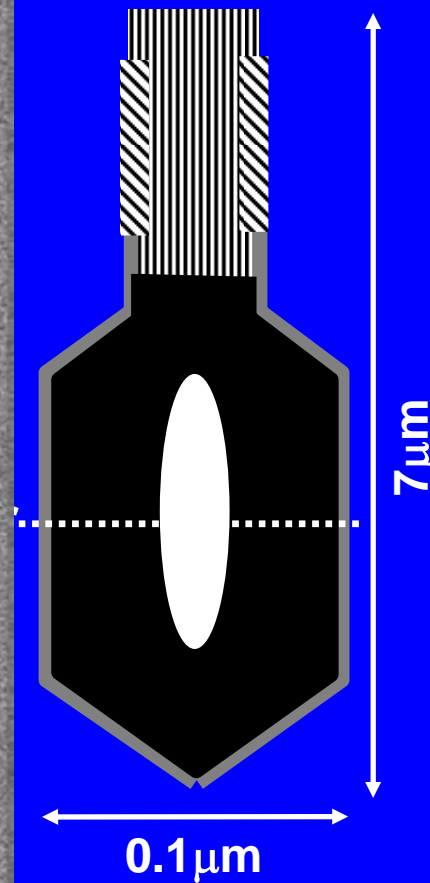
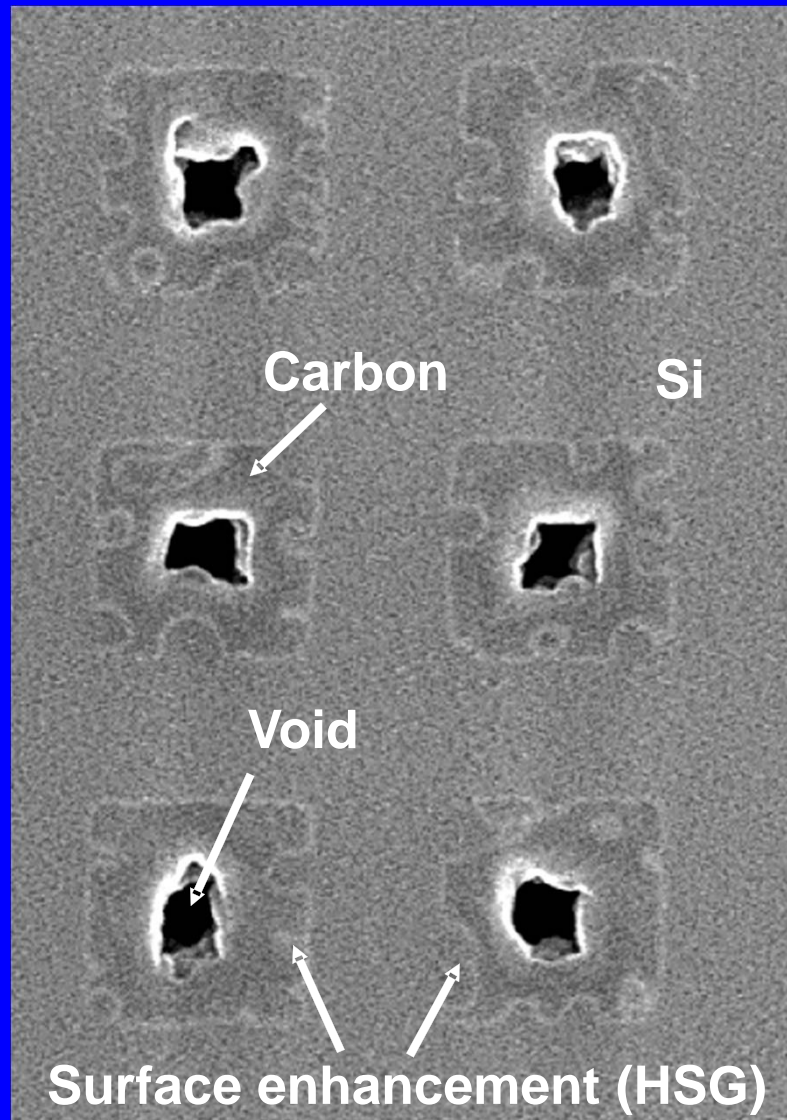
# Liner Top Electrode



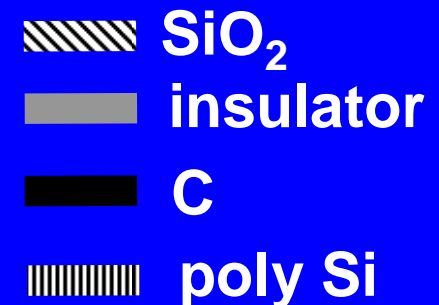
- Carbon liner as top electrode
- Conductivity gain
- No depletion (Capa gain)



# Bulk Top Electrode



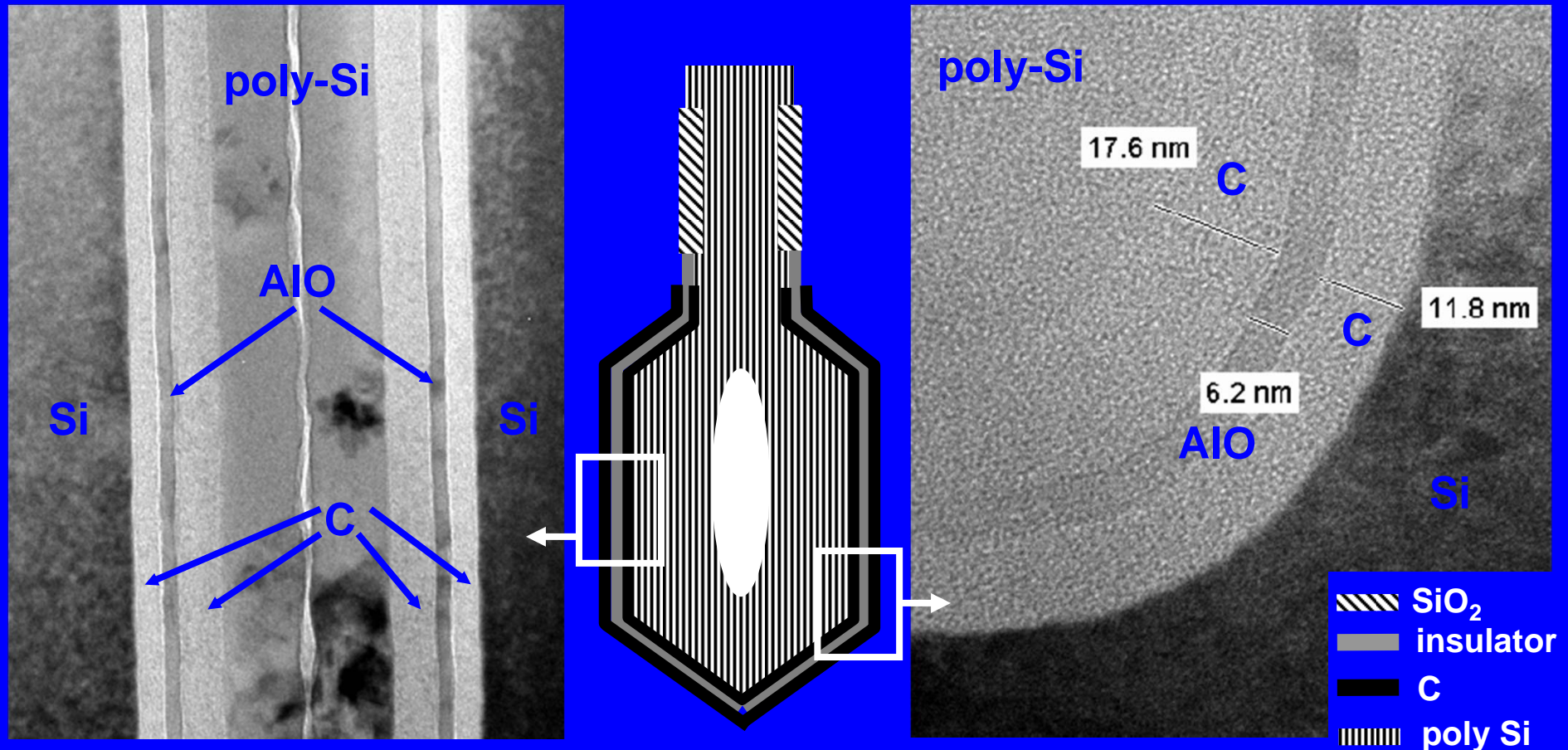
- Maximum conductivity gain
- Complexity reduction → no poly fill





# MIM Application

- C liner top and bottom electrode with high-k
- No depletion for pos. and neg. polarity

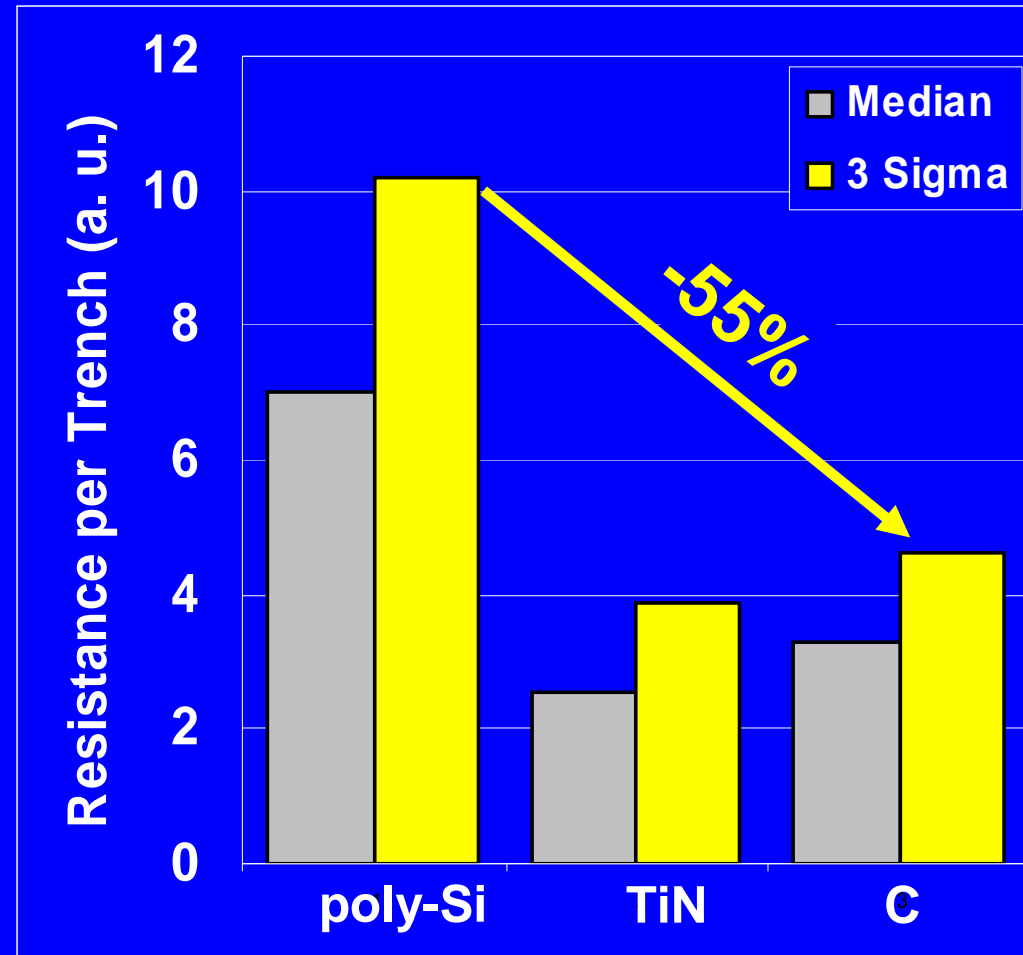
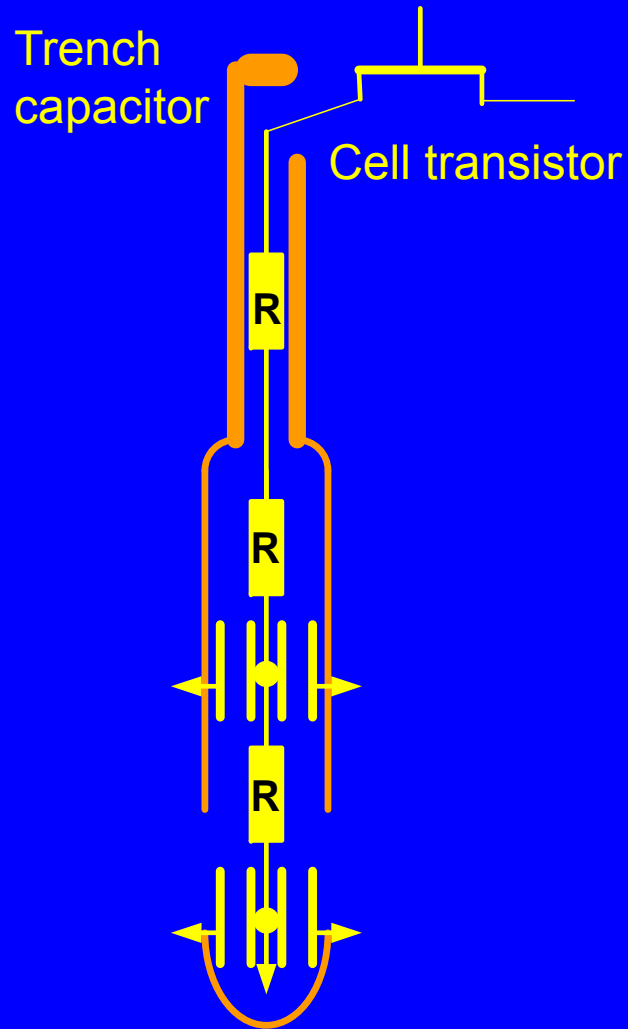




# Outline of Presentation

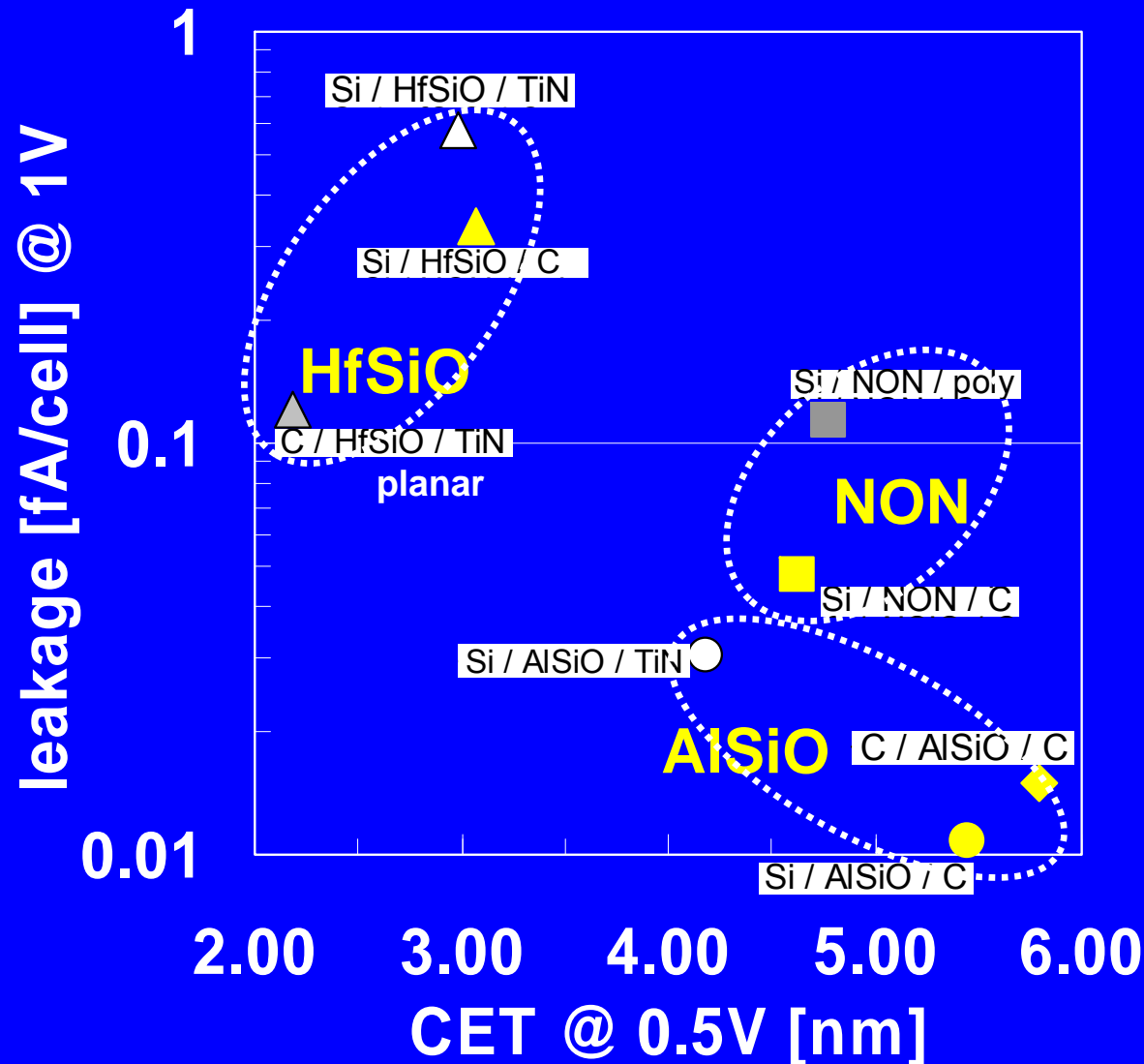
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# Electrical Resistivity



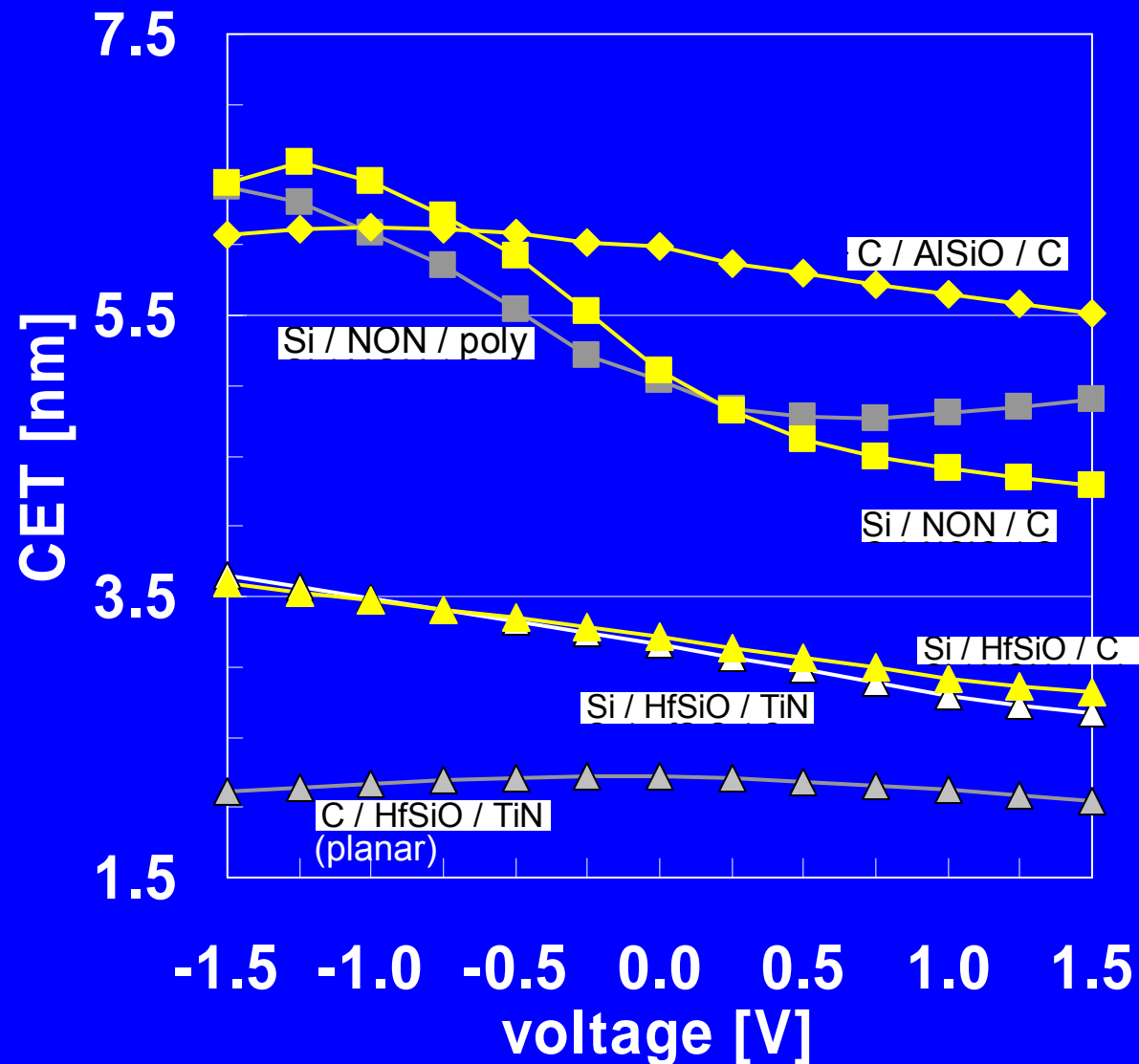
>50% resistance benefit with Carbon liner application

# CET Performance after 1050°C



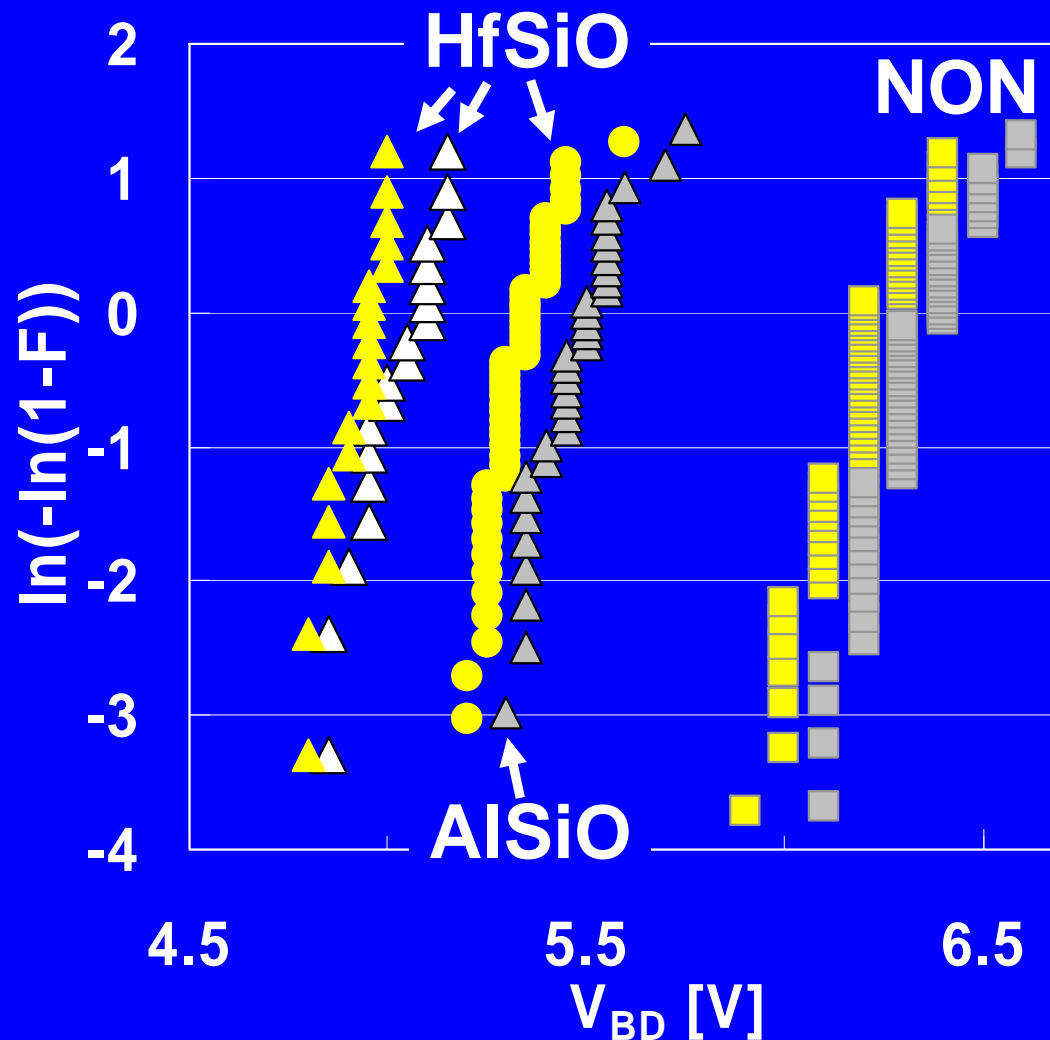
- CET ~2 w/ planar C/HfSiO/TiN MIM structure
- CET ~3 with C trench top electrode
- NON/C has lower leakage than NON/Si

# CET vs. Voltage



- Carbon MIS and MIM application is equivalent to TiN
- Carbon with NON shows capacitance benefit to poly-Si

# Breakdown Voltage - Reliability after 1050°C



- Carbon on NON has same  $V_{BD}$  as w/ poly
- High-k  $V_{BD}$  similar with C and TiN
- All options pass reliability

# Summary

- **Successful integration of Carbon as a cost effective enabler of sub 60nm DRAM generations has been demonstrated**
- **Carbon is employed as metallic top and bottom electrode in the Deep Trench Capacitor**
- **Using standard NON or high-k dielectrics at thermal budgets exceeding 1000°C**

# Acknowledgements

- Thanks to all the co-workers at Qimonda Dresden and Munich who greatly contributed to the success of this work
- This work was supported by the Ministry of Education and Research of the Federal Republic of Germany (project number 01M3171A)

