A novel reconfigurable silicon nanowire transistor

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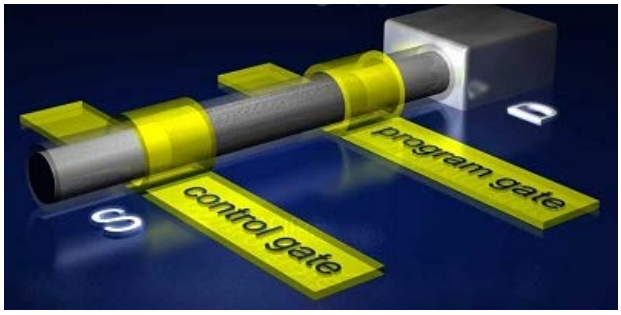
In a recently published paper, researchers report the development of a novel type of nano-transistors which are based on individually gated nanometer scale nanowire heterojunctions where electrons and holes are filtered selectively.

Electronic applications are dominated by Complementary Metal Oxide Semiconductor (CMOS) circuits which combine two different types of transistors (p- and n-type) to reduce power dissipation. Until now, these transistors provide static electrical functions. P- or n-type operation results from specific doping predetermined by fabrication processing and cannot be changed. Future electronic computing devices targeted as CMOS successors are expected to provide functional diversification while maintaining reasonable energy consumption.

The research report was published in a recent issue of the peer-reviewed journal Nano Letters. In this paper, Walter M. Weber and André Heinzig from Namlab in Germany (Dresden) have introduced and demonstrated experimentally a novel type of nano-transistors that addresses these demands.



Schematic of a reconfigurable silicon nanowire field effect transistor (RFET).
The program gate is used to select the p- or n-polarity whereas the control gate tunes the conductance through the nanowire. Image credit and copyright: Heinzig and Weber.

The capability to configure electronics for customized functions after manufacturing is provided by reprogrammable circuits. The reconfigurable nanowire field effect transistors (RFETs) exhibit electrical characteristics that can be reversibly programmed during operation. A single device provides the functionality of both types of field effect transistors (p- and n-type) required to build low energy consumption logic circuits.

The concept is enabled by employing an axial nanowire heterostructure (metal/intrinsic-silicon/metal) with a diameter of 20 nm embedded in silicon oxide shell (10 nm) and two independently working top gates as seen in the image above.

The fundamental effect that enables reconfigurability is the selective

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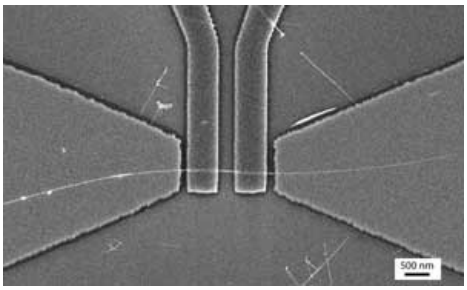
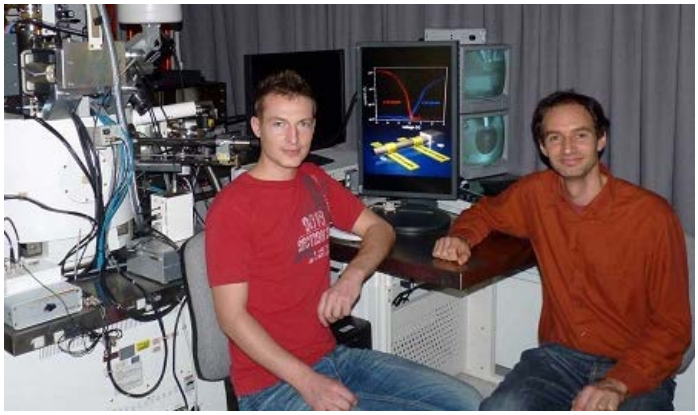
charge carrier transport through the two individually gated nanometer-scale Schottky junctions of the nanowire. One gate is used to block the undesired charge carrier type, while the other gate controls the injection of the desired carriers into the active region with high sensitivity.



SEM of a RFET with gate electrodes at the Schottky junctions of the nanowire. Image credit and copyright: Heinzig and Weber.

The realized concept of reconfigurability enhances electrical characteristics providing record on/off values (up to 1 x E9) of silicon nanowire devices and significantly reducing the source - drain leakage currents, compared to conventional field effect transistors.

The device physics of the RFET have been elucidated through measurements and supported by device simulations. The authors verified that the drive current for both p- and n-operation is significantly dominated by tunneling, which can be attributed to the geometry of the nanowire and the nanometer scale Schottky junctions.



Walter M. Weber (Right) , André Heinzig (Left). Image credit and copyright: Heinzig and Weber.

The fact that the semiconductor nanowires used do not need dopants gives this method a unique technological advantage. Accordingly, the devices are not vulnerable to typical performance constraints linked to dopant variability in nanoscale-semiconductor systems. Moreover, the technology can be transferred to other semiconductor materials and silicon-on-insulator (SOI) substrates principally enabling its implementation in an industrial environment.

An opposite biasing of the gates enables a “virtual band widening” for the injection of charge carriers from both electrodes. This state is unfeasible in conventional transistors. This results in negligible off-currents and makes the RFET concept especially promising for the implementation of low bandgap semiconductor materials, in which high junction leakage currents could be effectively suppressed.

The RFETs could replace common p- and n-type FETs to enable any boolean logic function in a complementary design. Thus, they are universal FETs for logic applications. Furthermore, the potential to change the n-type / p-type polarity of each transistor within the circuit enables the reconfiguration of this circuit. Specific logic functions can be dynamically

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altered during operation. Consequently, the main advantage of the concept is that additional logic functions can be provided with the same number of transistors compared to standard CMOS logic.

Science Story Reference:

Reconfigurable Silicon Nanowire Transistors. André Heinzig, Stefan Slesazeck, Franz Kreupl, Thomas Mikolajick, and Walter M. Weber. Nano Lett., Publication Date (Web): November 23, 2011. DOI: 10.1021/nl203094h

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