



Ambipolar Nanowire FETs: The phenomenon of ambipolar conduction (ability to switch between N- or P-type) has been observed in some nanoscale transistors made from silicon, carbon and graphene. While it is typically considered a limitation for circuit design at the 22nm node and below, a team led by researchers from the Swiss Federal Institute of Technology in Lausanne (EPFL) decided to try to exploit this property. They built gate-all-around ambipolar Si nanowire FETs in a vertically stacked configuration on an SOI substrate. A “polarity gate” attached to the ends of the nanowires is used to switch their polarity dynamically between the N and P states, while a control gate in the middle turns them on or off. The devices showed an excellent on/off current ratio of 10^6 and subthreshold slope of 70mV/dec. The researchers built a logic gate (the XOR function) to show the technique’s usefulness for future logic design.

The image at top left is a 3D view of the complete device.

The image at top right is a tilted SEM (scanning electron microscope) view of the nanowire stacks after deposition and etching of the polarity gate structures.

The image on the bottom is a computer simulation showing the structure of the optimized ambipolar silicon nanowire device structure, with three 45-nm-long gate regions.

(Paper #8.4, “Polarity Control in Double-Gate, Gate-All-Around Vertically Stacked Silicon Nanowire FETs,” M. De Marchi et al, EPFL)